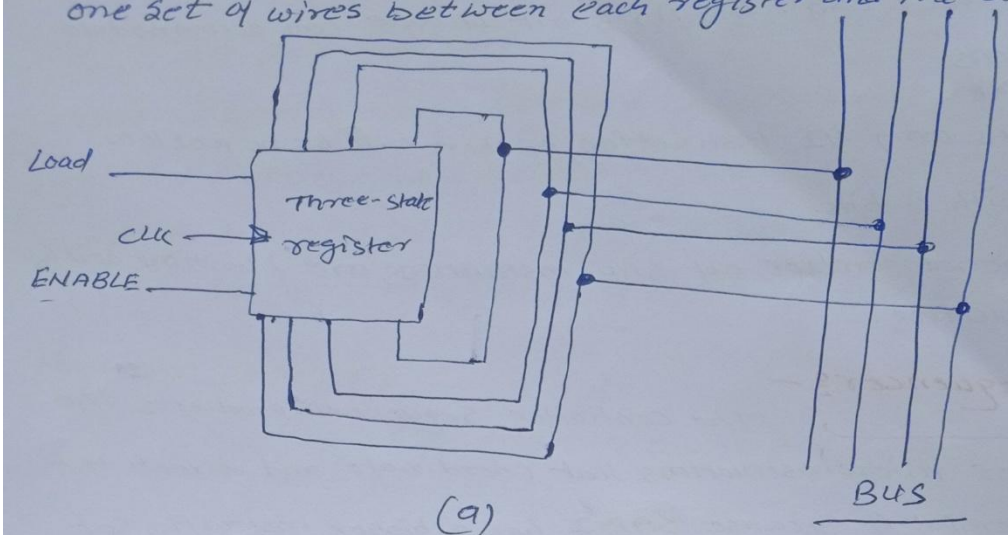
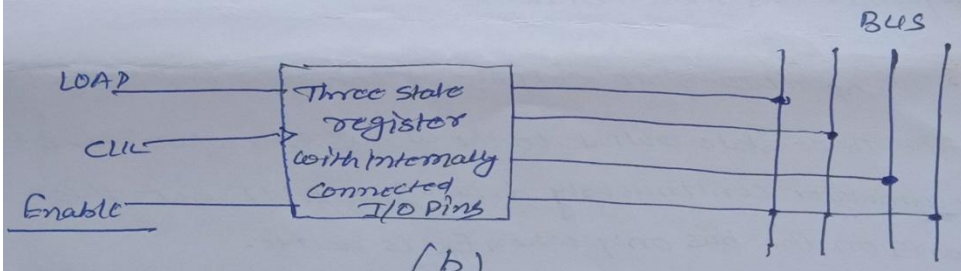
Bidirectional Registers :

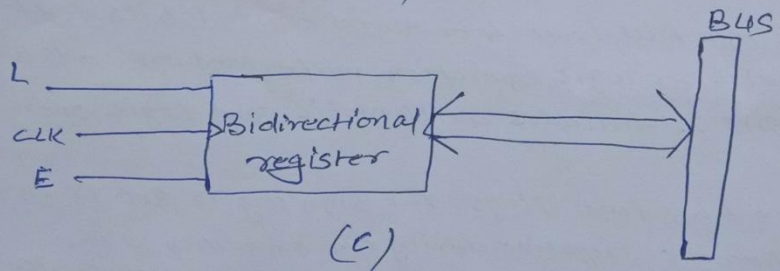
To reduce the wiring capacitance of SAP-2, we will run only one set of wires between each register and the bus.



(a)



(b)



(c)

Fig - Bidirectional register

Fig (a) shows the input and output pin are shorted; only one group of wires is connected to the bus. During a computer run, either LOAD or ENABLE may be active, but not both at the same time.

An active LOAD means that a binary word flows from the bus to the register input; during a load operation, the output line are floating.

An active ENABLE means that a binary word flows from the register to the bus; in this case, the input lines float.

Fig (b) shows the IC manufacturer can internally connect the input and output pins of a three-state register. This is not only reduces the wiring capacitance; it also reduces the number of I/O pins.

Fig (c) shows the symbol for a three-state register with internally connected input and output pins. The double headed arrow is that the path is bidirectional store data in

Explain the Architecture of SAP-2 with help of block diagram

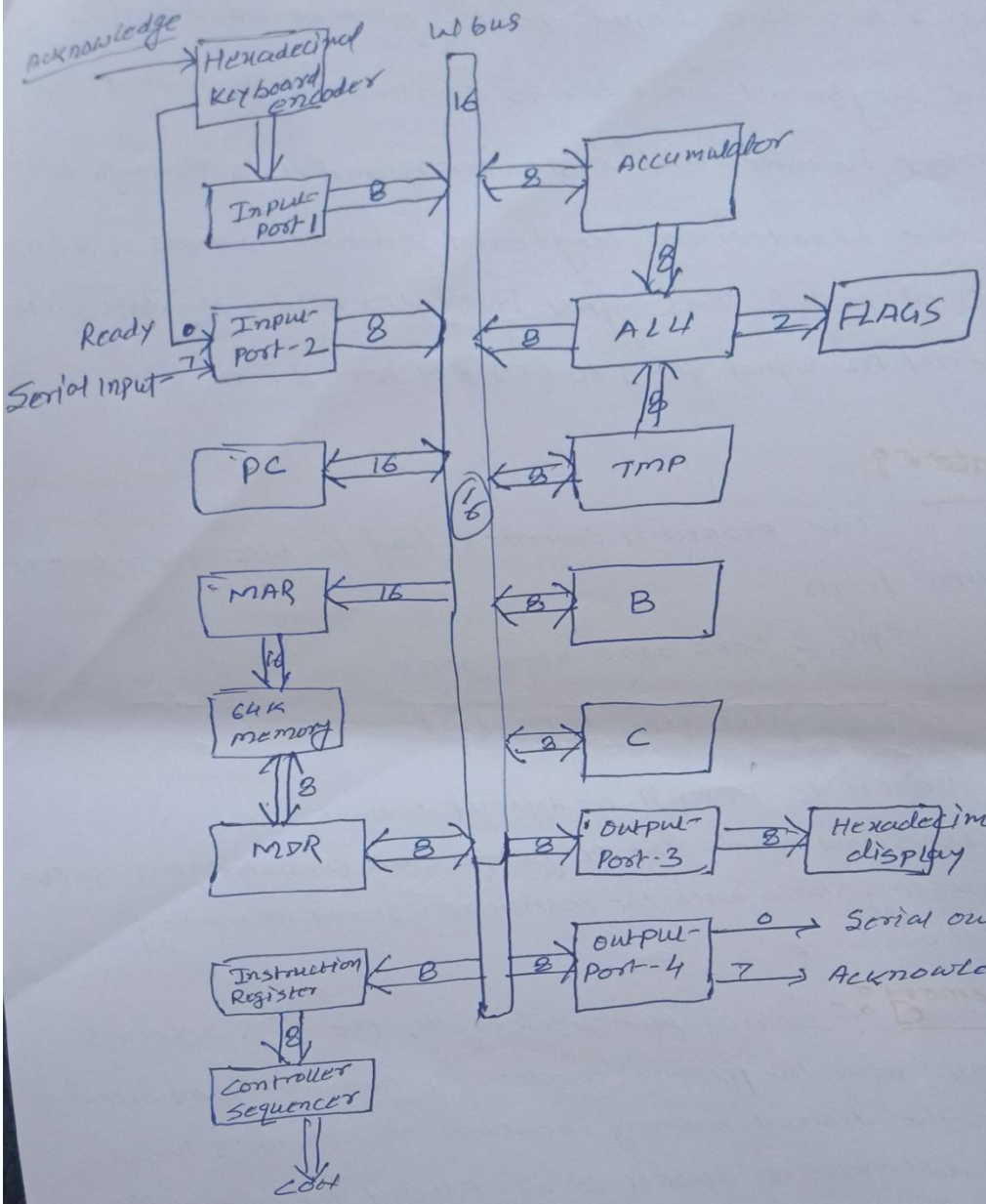


Fig.-1 SAP-2 Block diagram, Architecture

Fig. shows the architecture of SAP-2. All register connected outputs to the W-bus are three-state.

A brief description of each box is given now.

Input ports:

SAP-2 has two input ports, numbered 1 and 2. The hexadecimal keyboard encoder is connected to port 1. It allows us to enter hexadecimal instructions and data through port 1. Notice that the hexadecimal keyboard encoder sends a READ signal to bit 0 of port 2. This signal indicates when the data in Port is valid. Also serial IN signal going to Pin 7 of port 2.

Program Counter:

The program counter has 16 bits: therefore, it can count from

PC = 0000 0000 0000 0000

to

PC = 1111 1111 1111 1111

or

0000H to FFFFH or decimal 0 to 65,535.

A low $\overline{CLR}$ signal resets the PC before each computer run! So the data processing starts with the instruction stored in memory location 0000H.

MAR and memory:-

During the fetch cycle, the MAR receives 16 bit address from the program counter. The two state MAR output then addresses the desired memory location. The memory has a 2k ROM with addresses of 0000H to 07FFH and the rest of the memory is a 62K RAM with addresses from 0800H to FFFFH

Memory Data Register:

The memory data register (MDR) is an 8-bit buffer register. Its output Setup the RAM. The memory data register receives data from the bus before a write operation, and it sends data to the bus after a read operation.