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Lecture for M.Sc. Physics, II Semester Students

M.Sc. II Semester (Electronics Device)

Paper - IV, Unit – III, **Oscillators and Multivibrator**

OSCILLATION WITH *RC* FEEDBACK CIRCUITS

- There are three types of feedback oscillators that use RC circuits to produce sinusoidal outputs are the
  - **Wien-bridge oscillator**
  - **Phase-shift oscillator**
  - **Twin-T oscillator**
- Generally, RC feedback oscillators are used for frequencies up to about **1 MHz**.
- The Wien-bridge is by far the most widely used type of RC feedback oscillator for this range of frequencies.

Wien-Bridge Oscillator

- One type of sinusoidal feedback oscillator is the Wien-bridge oscillator.
- A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Figure 6(a).
- R_1 and C_1 together form the lag portion of the circuit; R_2 and C_2 form the lead portion.
- The operation of this lead-lag circuit is as follows.
  - At lower frequencies, the lead circuit takes over due to the high reactance of C_2.
  - As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase.
  - At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1} causes the output voltage to decrease.

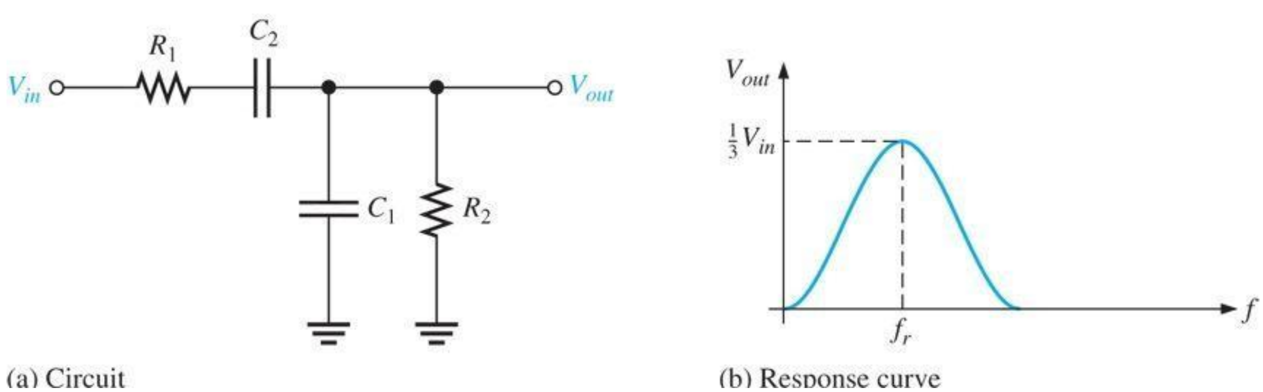

Figure 6 A lead-lag circuit and its response curve.

- The response curve for the lead-lag circuit shown in Figure 6(b) indicates that the output voltage peaks at a frequency called the **resonant frequency**, f_r.
- At this point, the attenuation (V_{out} / V_{in}) of the circuit is 1/3 if R_1=R_2 and X_{C1}= X_{C2} as stated by the following equation

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

- The formula for the resonant frequency is

$$f_r = \frac{1}{2\pi RC}$$

- To summarize, the lead-lag circuit in the Wien-bridge oscillator has a resonant frequency, f_r , at which the phase shift through the circuit is 0^0 and the attenuation is 1/3 .
- Below f_r, the lead circuit dominates and the output leads the input.
- Above f_r, the lag circuit dominates and the output lags the input.

The Basic Circuit

- The lead-lag circuit is used in the positive feedback loop of an op-amp, as shown in Figure 7(a).
- A voltage divider is used in the negative feedback loop.
- The Wien-bridge oscillator circuit can be viewed as a noninverting amplifier configuration with the input signal fed back from the output through the lead-lag circuit.
- Recall that the voltage divider determines the closed-loop gain of the amplifier.

$$A_{cl} = \frac{1}{B} = \frac{1}{R_2/(R_1+R_2)} = \frac{R_1+R_2}{R_2}$$

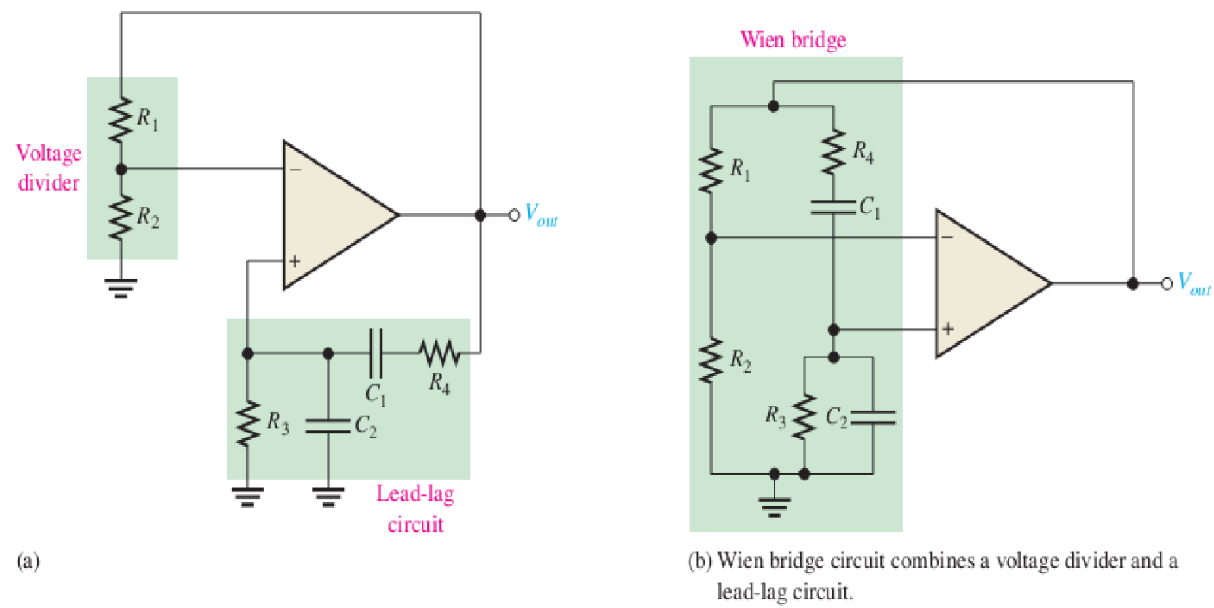

Figure 7 The Wien-bridge oscillator schematic drawn in two different but equivalent ways.

- The circuit is redrawn in Figure 7(b) to show that the op-amp is connected across the bridge circuit.
- One leg of the bridge is the lead-lag circuit, and the other is the voltage divider.

Positive Feedback Conditions for Oscillation

- As you know, for the circuit output to oscillate, the phase shift around the positive feedback loop must be 0° and the gain around the loop must equal unity (1).
- The 0° phase-shift condition is met when the frequency is f_r because the phase shift through the lead-lag circuit is 0° and there is no inversion from the noninverting input of the op-amp to the output.
- This is shown in Figure 8(a).

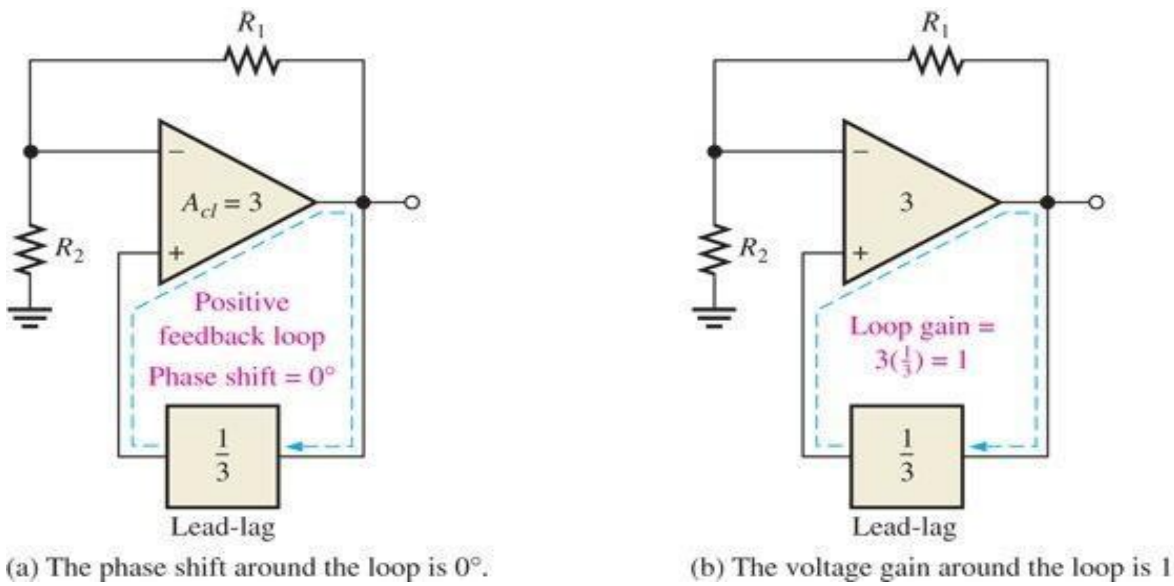

Figure 8 Conditions for sustained oscillation.

- The unity-gain condition in the feedback loop is met when $A_{cl} = 3$
- This offsets the 1/3 attenuation of the lead-lag circuit, thus making the total gain around the positive feedback loop equal to 1, as shown in Figure 8(b).
- To achieve a closed-loop gain of 3, $R_1 = 2R_2$

Start-Up Conditions

- Initially, the closed-loop gain of the amplifier itself must be more than 3 ($A_{cl} > 3$) until the output signal builds up to a desired level.
- Ideally, the gain of the amplifier must then decrease to 3 so that the total gain around the loop is 1 and the output signal stays at the desired level, thus sustaining oscillation.
- This is illustrated in Figure 9.

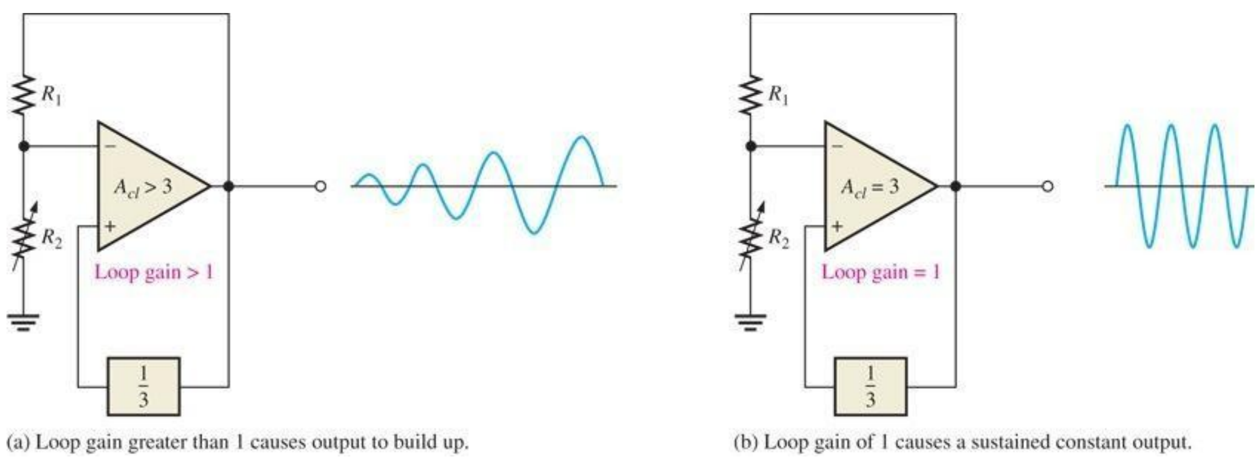

Figure 9 Conditions for start-up and sustained oscillations.

- The circuit in Figure 10 illustrates a method for achieving sustained oscillations.
- Notice that the voltage-divider circuit has been modified to include an additional resistor in parallel with a back-to-back zener diode arrangement.
- When DC power is first applied, both zener diodes appear as opens.
- This places R3 in series with R1 thus increasing the closed-loop gain of the amplifier as follows ($R_1 = 2R_2$)

$$A_{cl} = \frac{R_1 + R_2 + R_3}{R_2} = \frac{3R_2 + R_3}{R_2} = 3 + \frac{R_3}{R_2}$$

- Initially, a small positive feedback signal develops from noise.
- The lead-lag circuit permits only a signal with a frequency equal to f_r to appear in phase on the noninverting input.
- This feedback signal is amplified and continually strengthened, resulting in a buildup of the output voltage.
- When the output signal reaches the zener breakdown voltage, the zeners conduct and effectively short out R_3.
- This lowers the amplifier's closed-loop gain to 3.
- At this point, the total loop gain is 1 and the output signal levels off and the oscillation is sustained.
- A better method to control the gain uses a JFET as a voltage-controlled resistor in a negative feedback path.

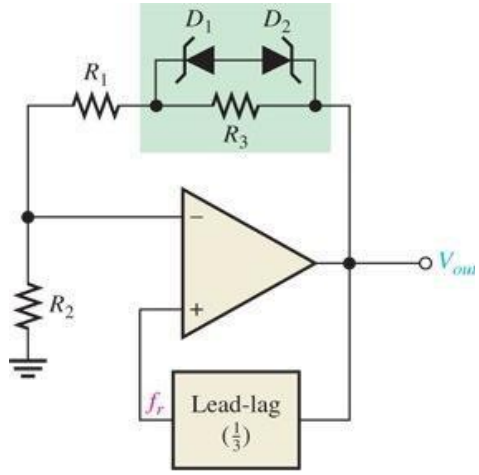

Figure 10 Self-starting Wien-bridge oscillator using back-to-back zener diodes.

- This method can produce an excellent sinusoidal waveform that is stable.
- A JFET operating with a small or zero V_{DS} is operating in the ohmic region.
- As the gate voltage increases, the drain-source resistance increases.
- If the JFET is placed in the negative feedback path, automatic gain control can be achieved because of this voltage-controlled resistance.

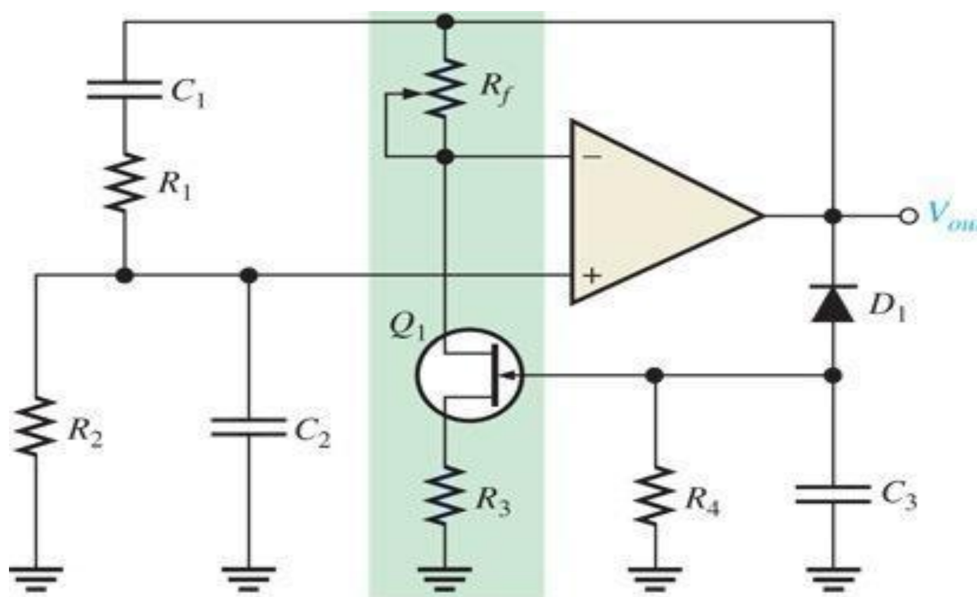

Figure 11 Self-starting Wien-bridge oscillator using a JFET in the negative feedback loop.

- A JFET stabilized Wien bridge is shown in Figure 11.
- The gain of the op-amp is controlled by the components shown in the green box, which include the JFET.
- The JFET's drain-source resistance depends on the gate voltage.
- With no output signal, the gate is at zero volts, causing the drain-source resistance to be at the minimum.
- With this condition, the loop gain is greater than 1.
- Oscillations begin and rapidly build to a large output signal.
- Negative output signal forward-bias D_1 causing capacitor C_3 to charge to a negative voltage.
- This voltage increases the drain-source resistance of the JFET and reduces the gain (and hence the output).
- With the proper selection of components, the gain can be stabilized at the required level.

To be contd. Next lecture