B-PSK

Binary Phase-Shift Keying

The simplest form of PSK is *binary phase-shift keying* (BPSK), where N = 1 and *M = 2*.

Therefore, with BPSK, two phases ($2^1 = 2$) are possible for the carrier.

One phase represents a logic 1, and the other phase represents a logic 0. As the input digital signal changes state (i.e., from a 1 to a 0 or from a 0 to a 1), the phase of the output carrier shifts between two angles that are separated by 180°.

Hence, other names for BPSK are *phase reversal keying* (PRK) and *biphase modulation.* BPSK is a form of square-wave modulation of a *continuous wave (CW)* signal.

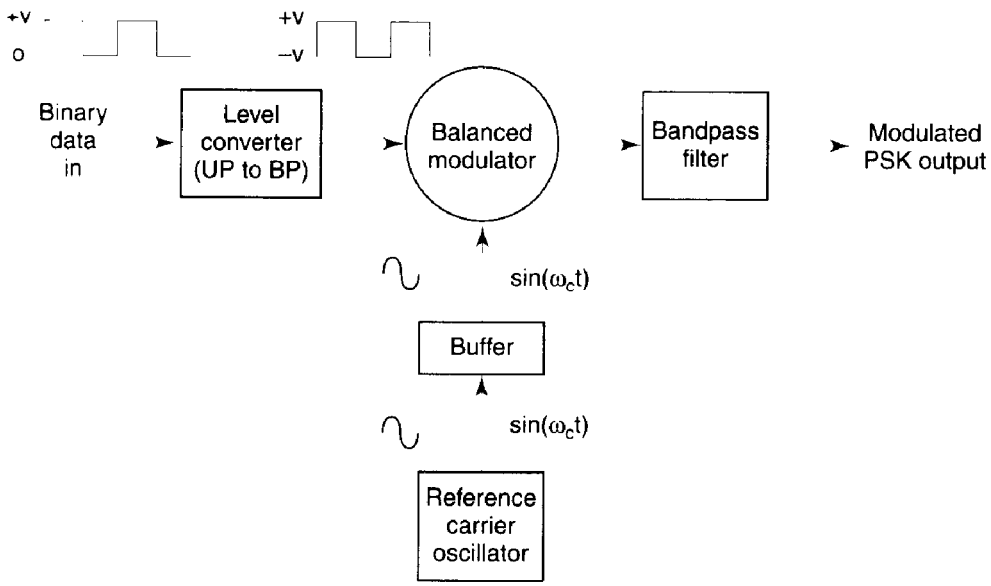


FIGURE 2-12 BPSK transmitter

BPSK transmitter.

Figure 2-12 shows a simplified block diagram of a BPSK transmitter.

The balanced modulator acts as a phase reversing switch. Depending on the logic condition of the digital input, the carrier is transferred to the output either in phase or 180° out of phase with the reference carrier oscillator.

Figure 2-13 shows the schematic diagram of a balanced ring modulator.

The balanced modulator has two inputs: a carrier that is in phase with the reference oscillator and the binary digital data.

For the balanced modulator to operate properly, the digital input voltage must be much greater than the peak carrier voltage.

This ensures that the digital input controls the on/off state of diodes D1 to D4. If the binary input is a logic 1(positive voltage), diodes D 1 and D2 are forward biased and on, while diodes D3 and D4 are reverse biased and off (Figure 2-13b). With the polarities shown, the carrier voltage is developed across transformer T2 in phase with the carrier voltage across T 1. Consequently, the output signal is in phase with the reference oscillator.

If the binary input is a logic 0 (negative voltage), diodes Dl and D2 are reverse biased and off, while diodes D3 and D4 are forward biased and on (Figure 9-13c). As a result, the carrier voltage is developed across transformer T2 180° out of phase with the carrier voltage across T 1.

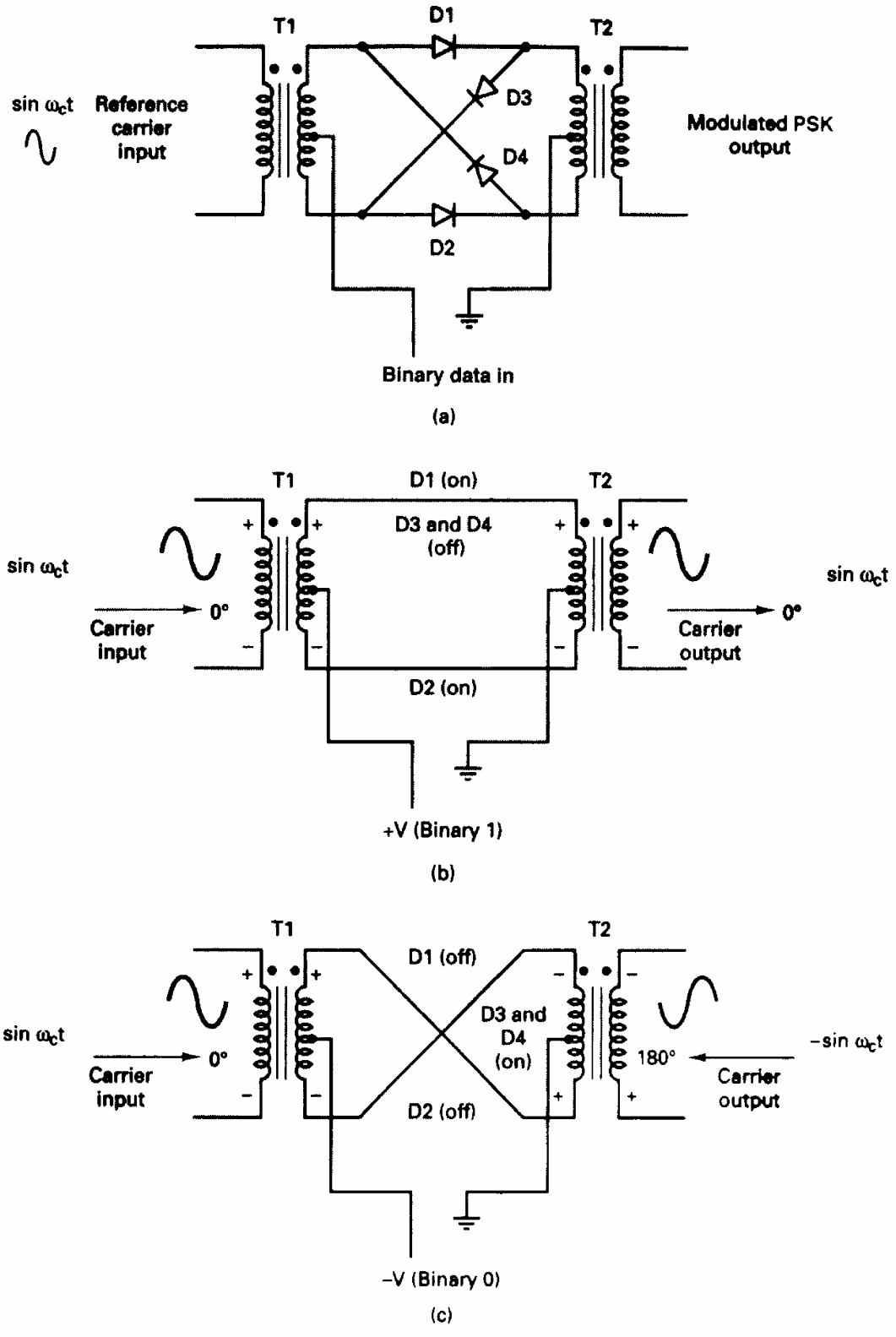


FIGURE 9-13 (a) Balanced ring modulator; (b) logic 1 input; (c) logic 0 input

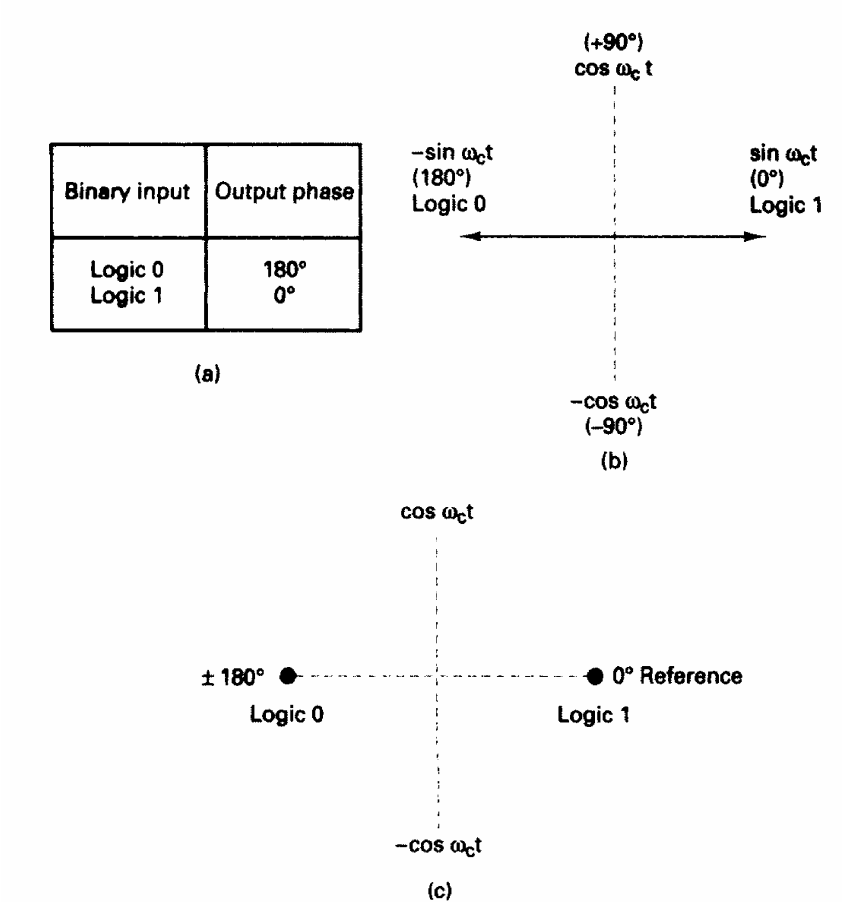


FIGURE 2-14 BPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

Bandwidth considerations of BPSK.

In a BPSK modulator. the carrier input signal is multiplied by the binary data.

If + 1 V is assigned to a logic 1 and -1 V is assigned to a logic 0, the input carrier (sin $\omega_c t$) is multiplied by either a + or - 1 .

The output signal is either + 1 sin $\omega_c t$ or -1 sin $\omega_c t$ the first represents a signal that is *in phase* with the reference oscillator, the latter a signal that is 180° out of phase with the reference oscillator.

Each time the input logic condition changes, the output phase changes.

Mathematically, the output of a BPSK modulator is proportional to

$$\text{BPSK output} = [\sin(2\pi f_a t)] \times [\sin(2\pi f_c t)] \qquad (2.20)$$

where
f_a = maximum fundamental frequency of binary input (hertz)
f_c = reference carrier frequency (hertz)

Solving for the trig identity for the product of two sine functions,

$$0.5\cos[2\pi(f_c - f_a)t] - 0.5\cos[2\pi(f_c + f_a)t]$$

Thus, the minimum double-sided Nyquist bandwidth *(B) is*

$$\begin{array}{r} f_c + f_a \\ -(f_c + f_a) \end{array} \qquad \text{or} \qquad \begin{array}{r} f_c + f_a \\ \underline{-f_c + f_a} \\ 2f_a \end{array}$$

and because $f_a = f_b / 2$, where f_b = input bit rate,
where *B is* the minimum double-sided Nyquist bandwidth.

Figure 2-15 shows the output phase-versus-time relationship for a BPSK waveform.

Logic 1 input produces an analog output signal with a 0° phase angle, and a logic 0 input produces an analog output signal with a 180° phase angle.

As the binary input shifts between a logic 1 and a logic 0 condition and vice versa, the phase of the BPSK waveform shifts between 0° and 180°, respectively.

BPSK signaling element (t_s) is equal to the time of one information bit (t_b), which indicates that the bit rate equals the baud.

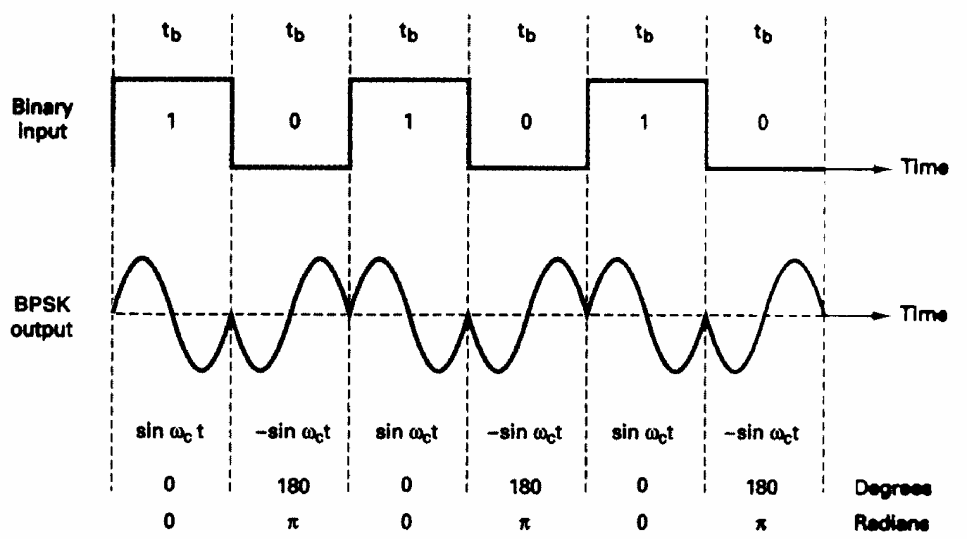


FIGURE 2-15 Output phase-versus-time relationship for a BPSK modulator

Example 2-4

For a BPSK modulator with a carrier frequency of 70 MHz and an input bit rate of 10 Mbps, determine the maximum and minimum upper and lower side frequencies, draw the output spectrum, determine the minimum Nyquist bandwidth, and calculate the baud..

Solution

Substituting into Equation 2-20 yields

output = [sin ($2\pi f_a t$)] x [sin ($2\pi f_c t$)] ; $f_a = f_b / 2 = 5$ MHz

= [sin 2π(5MHz)t)] x [sin 2π(70MHz)t)]

= 0.5cos[2π(70MHz – 5MHz)t] – 0.5cos[2π(70MHz + 5MHz)t]

lower side frequency upper side frequency

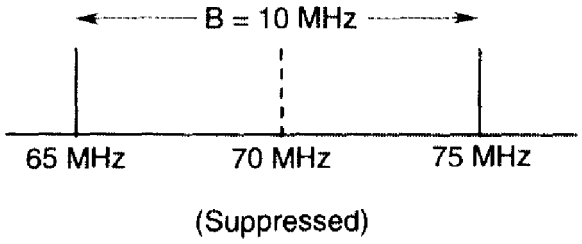
Minimum lower side frequency (LSF):

LSF=70MHz - 5MHz = 65MHz

Maximum upper side frequency (USF):

USF = 70 MHz + 5 MHz = 75 MHz

Therefore, the output spectrum for the worst-case binary input conditions *is* as follows: The minimum Nyquist bandwidth *(B) is*



B = 75 MHz - 65 MHz = 10 MHz

and the baud = f_b or 10 megabaud.

BPSK receiver.

Figure 2-16 shows the block diagram of a BPSK receiver.

The input signal maybe + sin $\omega_c t$ or - sin $\omega_c t$.

The coherent carrier recovery circuit detects and regenerates a carrier signal that is both frequency and phase coherent with the original transmit carrier.

The balanced modulator is a product detector; the output is the product d the two inputs (the BPSK signal and the recovered carrier).

The low-pass filter (LPF) operates the recovered binary data from the complex demodulated signal.

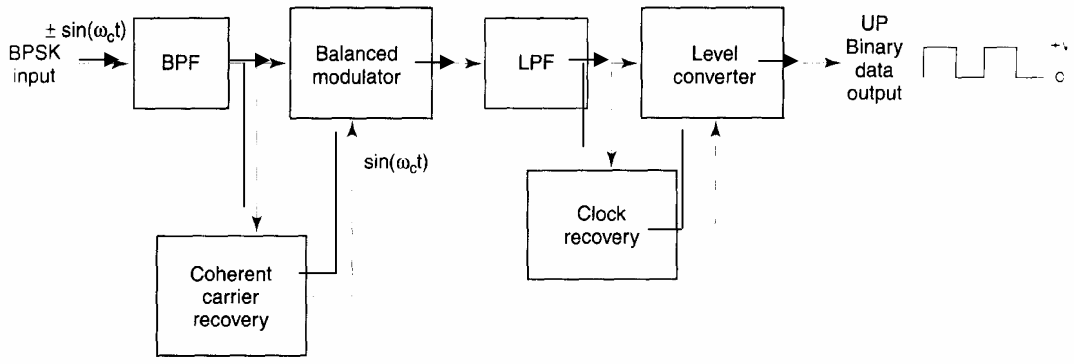


FIGURE 2-16 Block diagram of a BPSK receiver

Mathematically, the demodulation process is as follows.

For a BPSK input signal of + sin $\omega_c t$ (logic 1), the output of the balanced modulator is

$$\text{output} = (\sin \omega_c t)(\sin \omega_c t) = \sin^2 \omega_c t \qquad (2.21)$$

or

$$\sin^2 \omega_c t = 0.5(1 - \cos 2\omega_c t) = 0.5 - 0.5\cos 2\omega_c t$$

filtered out

leaving

$$\text{output} = +0.5 \text{ V} = \text{logic 1}$$

It can be seen that the output of the balanced modulator contains a positive voltage (+[1/2]V) and a cosine wave at twice the carrier frequency (2 $\omega_c t$).

The LPF has a cutoff frequency much lower than 2 $\omega_c t$, and, thus, blocks the second harmonic of the carrier and passes only the positive constant component. A positive voltage represents a demodulated logic 1.

For a BPSK input signal of -sin $\omega_c t$ (logic 0), the output of the balanced modulator is

$$\text{output} = (-\sin \omega_c t)(\sin \omega_c t) = \sin^2 \omega_c t$$

or

$$\sin^2 \omega_c t = -0.5(1 - \cos 2\omega_c t) = 0.5 + 0.5\cos 2\omega_c t$$

filtered out

leaving

output = - 0.5 V = logic 0

The output of the balanced modulator contains a negative voltage (-[l/2]V) and a cosine wave at twice the carrier frequency ($2\omega_c t$).

Again, the LPF blocks the second harmonic of the carrier and passes only the negative constant component. A negative voltage represents a demodulated logic 0.