# Module
## 1

# Power Semiconductor Devices

# Lesson
## 5

# Gate Turn Off Thyristor (GTO)

# Instructional objective

On completion the student will be able to

- Differentiate between the constructional features of a GTO and a Thyristor.

- Explain the turn off mechanism of a GTO.

- Differentiate between the steady state output and gate characteristics of a GTO and a thyristor.

- Draw and explain the switching characteristics of a GTO.

- Draw the block diagram of a GTO gate drive unit and explain the functions of different blocks.

- Interpret the manufacturer's data sheet of a GTO.

# Introduction

The thyristor has reigned supreme for well over two decades in the power electronics industry and continues to do so at the very highest level of power. It, however, has always suffered from the disadvantage of being a semi-controlled device. Although it could be turned on by applying a gate pulse but to turn it off the main current had to be interrupted. This proved to be particularly inconvenient in DC to AC and DC to DC conversion circuits, where the main current does not naturally becomes zero. A bulky and expensive "commutation circuit" had to be used to ensure proper turning off of the thyristor. The switching speed of the device was also comparatively slow even with fast inverter grade thyristor. The development of the Gate Turn off thyristor (GTO) has addressed these disadvantages of a thyristor to a large extent. Although it has made a rather late entry (1973) into the thyristor family the technology has matured quickly to produce device comparable in rating (5000V, 4000Amp) with the largest available thyristor. Consequently it has replaced the forced commutated inverter grade thyristor in all DC to AC and DC to DC converter circuits.

Like thyristor, the GTO is a current controlled minority carrier (i.e. bipolar) device. GTOs differ from conventional thyristor in that, they are designed to turn off when a negative current is sent through the gate, thereby causing a reversal of the gate current. A relatively high gate current is need to turn off the device with typical turn off gains in the range of 4-5. During conduction, on the other hand, the device behaves just like a thyristor with very low ON state voltage drop.

Several different varieties of GTOs have been manufactured. Devices with reverse blocking capability equal to their forward voltage ratings are called "symmetric GTOs". However, the most poplar variety of the GTO available in the market today has no appreciable reverse voltage (20-25v) blocking capacity. These are called "Asymmetric GTOs". Reverse conducting GTOs (RC-GTO) constitute the third family of GTOs. Here, a GTO is integrated with an anti-parallel freewheeling diode on to the same silicon wafer. This lesson will describe the construction, operating principle and characteristic of "Asymmetric GTOs" only.

## 5.2   Constructional Features of a GTO

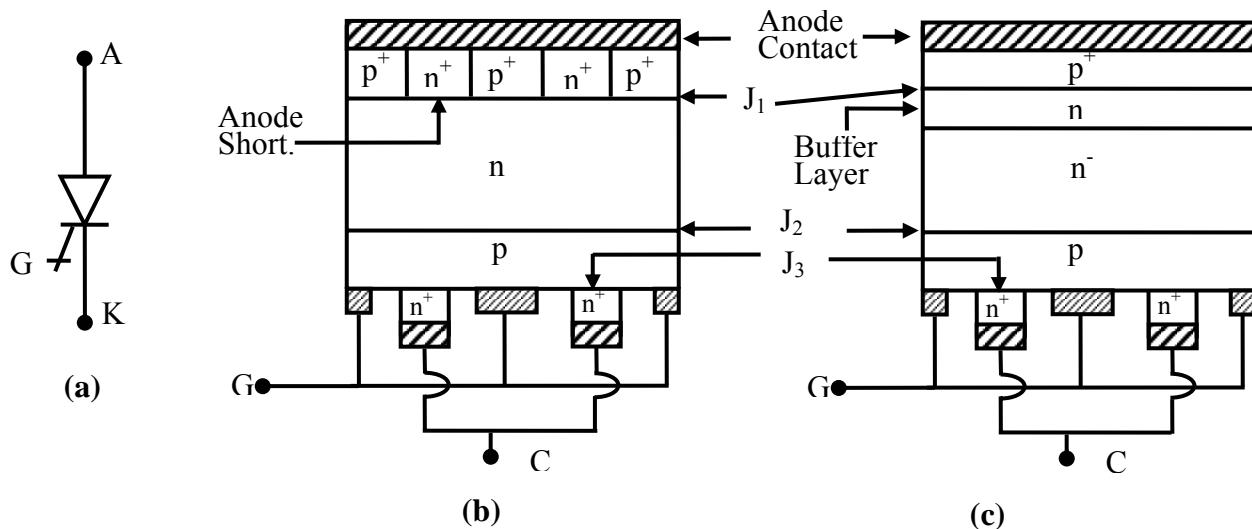Fig 5.1 shows the circuit symbol and two different schematic cross section of a GTO.

**Fig. 5.1: Circuit symbol and schematic cross section of a GTO**
**(a) Circuit Symbol, (b) Anode shorted GTO structure,**
**(c)  Buffer layer GTO structure.**

Like a thyristor, a GTO is also a four layer three junction **p-n-p-n** device. In order to obtain high emitter efficiency at the cathode end, the $\mathbf{n^+}$ cathode layer is highly doped. Consequently, the break down voltage of the function $J_3$ is low (typically 20-40V). The **p** type gate region has conflicting doping requirement. To maintain good emitter efficiency the doping level of this layer should be low, on the other hand, from the point of view of good turn off properties, resistively of this layer should be as low as possible requiring the doping level of this region to be high. Therefore, the doping level of this layer is highly graded. Additionally, in order to optimize current turn off capability, the gate cathode junction must be highly interdigitated. A 3000 Amp GTO may be composed of upto 3000 individual cathode segments which are a accessed via a common contact. The most popular design features multiple segments arranged in concentric rings around the device center.

The maximum forward blocking voltage of the device is determined by the doping level and the thickness of the **n** type base region next. In order to block several kv of forward voltage the doping level of this layer is kept relatively low while its thickness is made considerably higher (a few hundred microns). Byond the maximum allowable forward voltage either the electric field at the main junction ($J_2$) exceeds a critical value (avalanche break down) or the **n** base fully depletes, allowing its electric field to touch the anode emitter (punch through).

The junction between the **n** base and **p+** anode ($J_1$) is called the "anode junction". For good turn on properties the efficiency of this anode junction should be as high as possible requiring a heavily doped **p+** anode region. However, turn off capability of such a GTO will be poor with very low maximum turn off current and high losses. There are two basic approaches to solve this problem.

In the first method, heavily doped **n+** layers are introduced into the **p+** anode layer. They make contact with the same anode metallic contact. Therefore, electrons traveling through the base can directly reach the anode metal contact without causing hole injection from the **p+** anode. This is the classic "anode shorted GTO structure" as shown in Fig 5.1 (b). Due to presence of these "anode shorts" the reverse voltage blocking capacity of GTO reduces to the reverse break down

voltage of junction $J_3$ (20-40 volts maximum). In addition a large number of "anode shorts" reduces the efficiency of the anode junction and degrades the turn on performance of the device. Therefore, the density of the "anode shorts" are to be chosen by a careful compromise between the turn on and turn off performance.

In the other method, a moderately doped **n** type buffer layer is juxtaposed between the **n⁻** type base and the anode. As in the case of a power diode and BJT this relatively high density buffer layer changes the shape of the electric field pattern in the **n⁻** base region from triangular to trapezoidal and in the process, helps to reduce its width drastically. However, this buffer layer in a conventional "anode shorted" GTO structure would have increased the efficiency of the anode shorts. Therefore, in the new structure the anode shorts are altogether dispensed with and a thin **p+** type layer is introduce as the anode. The design of this layer is such that electrons have a high probability of crossing this layer without stimulating hole injection. This is called the "Transparent emitter structure" and is shown in Fig 5.1 (c).

**Exercise 5.1**

Fill in the blank(s) with the appropriate word(s)

  i.   A GTO is a _____ controlled _____ carrier device.

  ii.  A GTO has _____ layers and _____ terminals.

  iii. A GTO can be turned on by injecting a _____ gate current and turned off by

       injecting a _____ gate current.

  iv.  The anode shorts of a GTO improves the _____ performance but degrades

       the _____ performance.

  v.   The reverse voltage blocking capacity of a GTO is small due to the presence of

       _____.

**Answer:**  (i) current, minority; (ii) four, three; (iii) positive, negative; (iv) turn off, turn on; (v) anode shorts.

## 5.3  Operating principle of a GTO

GTO being a monolithic **p-n-p-n** structure just like a thryistor its basic operating principle can be explained in a manner similar to that of a thyristor. In particular, the **p-n-p-n** structure of a GTO can be though of consisting of one **p-n-p** and one **n-p-n** transistor connected in the regenerative configuration as shown in Fig 5.2.
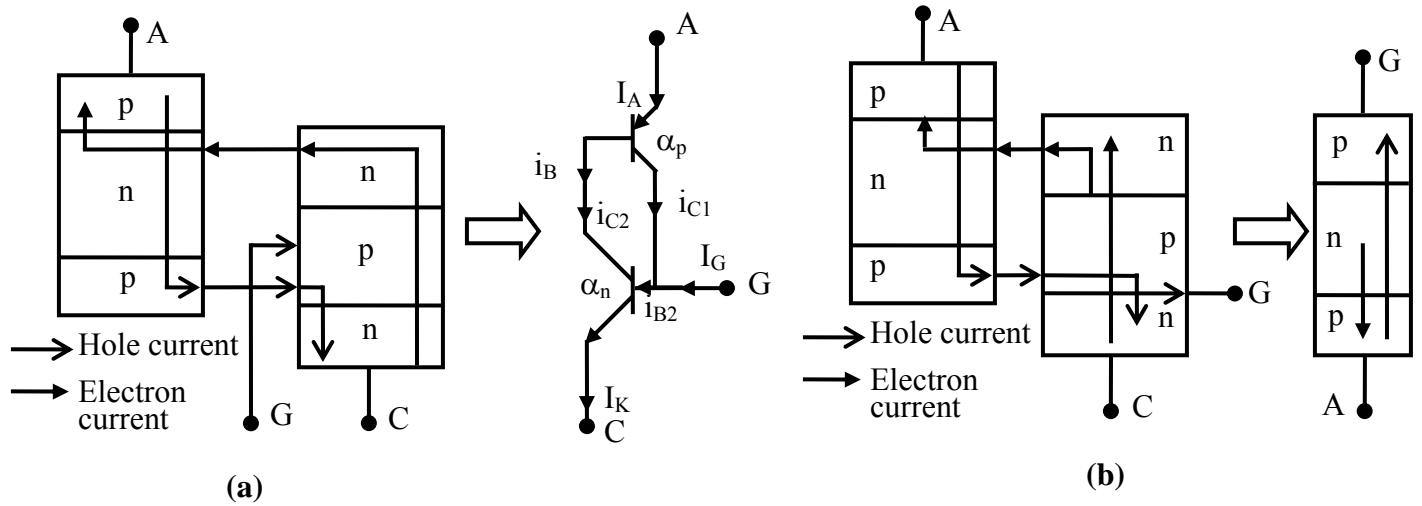
**Fig 5.2: Current distribution in a GTO**
**(a) During turn on; (b) During turn off.**

From the "two transistor analogy" (Fig 5.2 (a)) of the GTO structure one can write.

$$i_{C1} = \propto_p I_A + I_{CBO1} \qquad (5.1)$$

$$i_{B1} = i_{C2} = \propto_n I_k + I_{CBO2} \qquad (5.2)$$

$$I_k = I_A + I_G \quad \text{and} \quad I_A = i_{B1} + i_{C1} \qquad (5.3)$$

Combining $\quad I_A = \dfrac{\propto_n I_G + \left(i_{CBO1} + i_{CBO2}\right)}{1 - \left(\propto_n + \propto_p\right)} \qquad (5.4)$

With applied forward voltage $V_{AK}$ less than the forward break over voltage both $I_{CBO1}$ and $I_{CBO2}$ are small. Further if $I_G$ is zero $I_A$ is only slightly higher than $(I_{CBO1} + I_{CBO2})$. Under this condition both $\propto_n$ and $\propto_p$ are small and $(\propto_p + \propto_n) \ll 1$. The device is said to be in the forward blocking mode.

To turn the device on either the anode voltage can be raised until $I_{CBO1}$ and $I_{CBO2}$ increases by avalanche multiplication process or by injecting a gate current. The current gain $\propto$ of silicon transistors rises rapidly as the emitter current increases. Therefore, any mechanism which causes a momentary increase in the emitter current can be used to turn on the device. Normally, this is done by injecting current into the p base region via the external gate contract. As $\propto_n + \propto_p$ approaches unity the anode current tends to infinity. Physically as $\propto_n + \propto_p$ nears unity the device starts to regenerate and each transistor drives its companion into saturation. Once in saturation, all junctions assume a forward bias and total potential drop across the device becomes approximately equal to that of a single **p-n** diode. The anode current is restricted only by the external circuit. Once the device has been turned on in this manner, the external gate current is no longer required to maintain conduction, since the regeneration process is self-sustaining. Reversion to the blocking mode occurs only when the anode current is brought below the "holding current" level.

To turn off a conducting GTO the gate terminal is biased negative with respect to the cathode. The holes injected from the anode are, therefore, extracted from the p base through the gate metallization into the gate terminal (Fig 5.2 (b)). The resultant voltage drop in the **p** base above the **n** emitter starts reverse biasing the junction $J_3$ and electron injection stops here. The process originates at the periphery of the **p** base and the **n** emitter segments and the area still injecting electron shrinks. The anode current is crowded into higher and higher density filaments in most remote areas from the gate contact. This is the most critical phase in the GTO turn off process since highly localized high temperature regions can cause device failure unless these current filaments are quickly extinguished. When the last filament disappears, electron injection stops completely and depletion layer starts to grow on both $J_2$ and $J_3$. At this point the device once again starts blocking forward voltage. However, although the cathode current has ceased the anode to gate current continues to flow (Fig 5.2 (b)) as the **n** base excess carriers diffuse towards $J_1$. This "tail current" then decays exponentially as the **n** base excess carriers reduce by recombination. Once the tail current has completely disappeared does the device regain its steady state blocking characteristics. "Anode Shorts" (or transparent emitter) helps reduce the tail current faster by providing an alternate path to the **n** base electrons to reach the anode contact without causing appreciable hole injection from anode.

**Exercise 5.2**

Fill in the blank(s) with the appropriate word(s)

  i.   After a GTO turns on the gate current can be _____.

  ii.  A conducting GTO reverts back to the blocking mode when the anode current falls below _____ current.

  iii. To turn off a conducting GTO the gate terminal is biased _____ with respect to the _____.

  iv.  "Current filaments" produced during the turn off process of a GTO can destroy the device by creating local _____.

  v.   "Anode shorts" help to reduce the _____ current in a GTO.

**Answer:**  (i) removed; (ii) holding; (iii) negatively, cathode; (iv) hot spot; (v) tail.

## 5.4   Steady state and dynamic characteristics of a GTO

## 5.4.1 Steady state output and gate characteristics



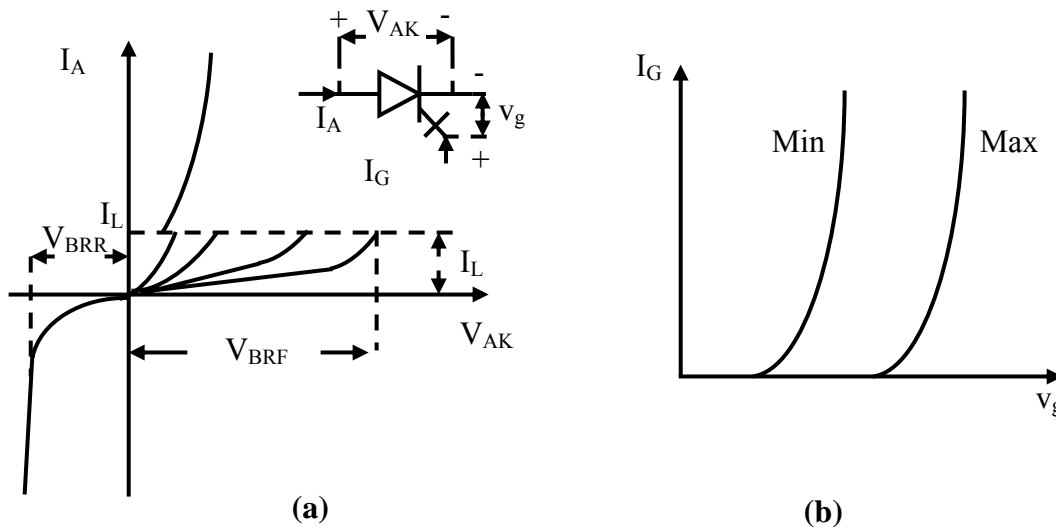(a)                                                (b)

**Fig. 5.3:   Steady state characteristics of a GTO**
**(a)  Output characteristics;  (b)  Gate characteristics.**

This characteristic in the first quadrant is very similar to that of a thyristor as shown in Fig. 5.3 (a). However, the latching current of a GTO is considerably higher than a thyristor of similar rating. The forward leakage current is also considerably higher. In fact, if the gate current is not sufficient to turn on a GTO it operates as a high voltage low gain transistor with considerable anode current. It should be noted that a GTO can block rated forward voltage only when the gate is negatively biased with respect to the cathode during forward blocking state. At least, a low value resistance must be connected across the gate cathode terminal. Increasing the value of this resistance reduces the forward blocking voltage of the GTO. Asymmetric GTOs have small (20-30 V) reverse break down voltage. This may lead the device to operate in "reverse avalanche" under certain conditions. This condition is not dangerous for the GTO provided the avalanche time and current are small. The gate voltage during this period must remain negative.

Fig 5.3 (b) shows the gate characteristics of a GTO. The zone between the min and max curves reflects parameter variation between individual GTOs. These characteristics are valid for DC and low frequency AC gate currents. They do not give correct voltage when the GTO is turned on with high $dia/dt$ and $dI_G/dt$. $V_G$ in this case is much higher.
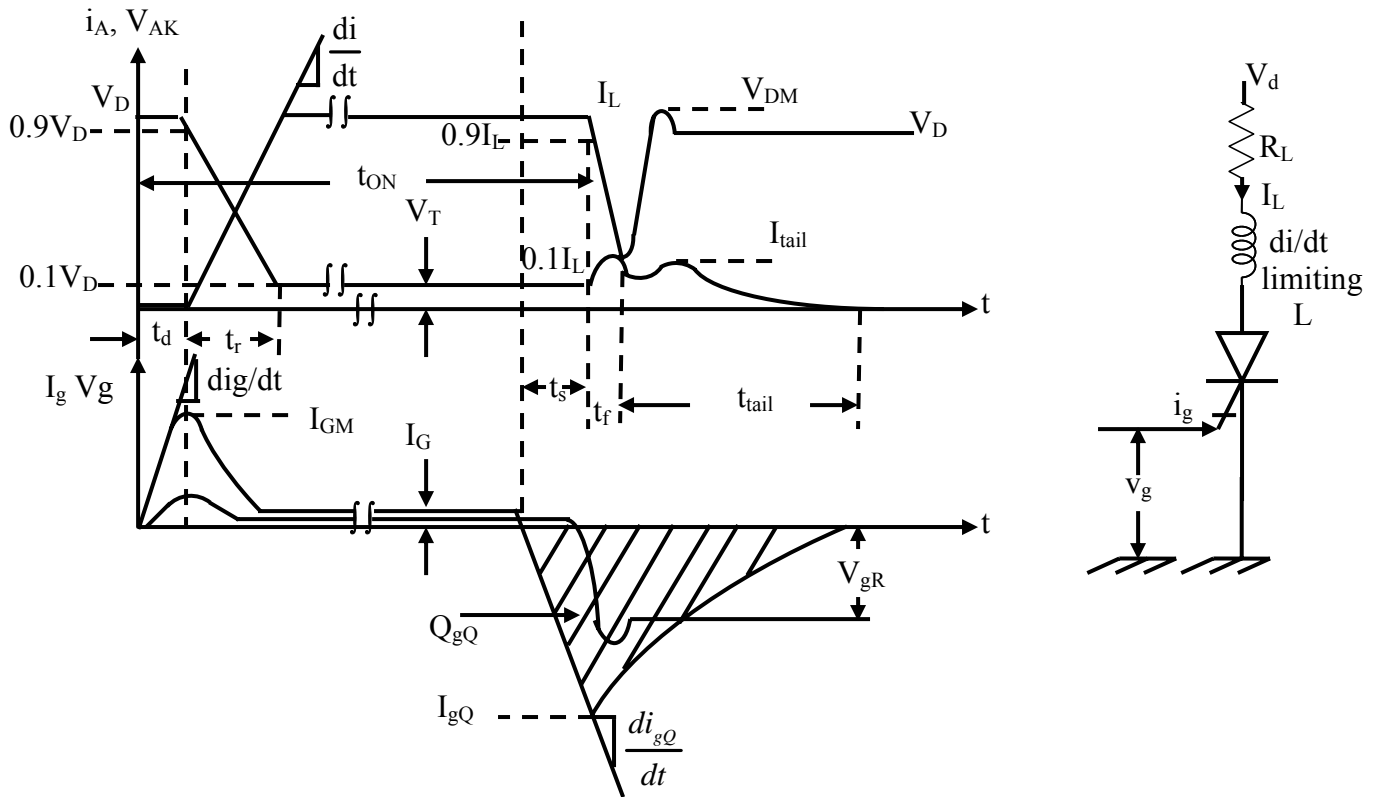
## 5.4.2 Dynamic characteristics of a GTO



**Fig. 5.4: Switching characteristics of a GTO.**

Fig 5.4 shows the switching characteristics of a GTO and refers to the resistive dc load switching circuit shown on the right hand side. When the GTO is off the anode current is zero and $V_{AK} = V_d$. To turn on the GTO, a positive gate current pulse is injected through the gate terminal. A substantial gate current ensure that all GTO cathode segments are turned on simultaneously and within a short time. There is a delay between the application of the gate pulse and the fall of anode voltage, called the turn on delay time $t_d$. After this time the anode voltage starts falling while the anode current starts rising towards its steady value $I_L$. Within a further time interval $t_r$ they reach 10% of their initial value and 90% of their final value respectively. $t_r$ is called the current rise time (voltage fall time). Both $t_d$ and maximum permissible on state $\frac{di_A}{dt}$ are very much gate current dependent. High value of $I_{gM}$ and $\frac{dig}{dt}$ at turn on reduces these times and increases maximum permissible on state $\frac{di_A}{dt}$. It should be noted that large value of $i_g$ ($I_{gM}$) and $\frac{dig}{dt}$ are required during $t_d$ and $t_r$ only. After this time period both $v_g$ and $i_g$ settles down to their steady value. A minimum ON time period $t_{ON}$ (min) is required for homogeneous anode current conduction in the GTO. This time is also necessary for the GTO to be able to turn off its rated anode current.

To turn off a GTO the gate terminal is negatively biased with respect to the cathode. With the application of the negative bias the gate current starts growing in the negative direction. However, the anode voltage,current or the gate voltage does not change appreciably from their on state levels for a further time period called the storage time ($t_s$). The storage time increases with the turn off anode current and decrease with $di_{gQ}/dt$. During storage time the load current at the cathode end is gradually diverted to the gate terminal. At the end of the storage time gate current reaches its negative maximum value $I_{gQ}$. At this point both the junctions $J_2$ & $J_3$ of the GTO starts blocking voltage. Consequently, both the gate cathode and the anode cathode voltage starts rising towards their final value while the anode current starts decreasing towards zero. At the end of current fall time "$t_f$" the anode current reaches 10% of its initial value after which both the anode current and the gate current continues to flow in the form of a current tail for a further duration of $t_{tail.}$ A GTO is normally used with a R-C turn off snubber. Therefore, $V_{AK}$ does not start to rise appreciably till $t_f$. At this point $V_{AK}$ starts rising rapidly and exceeds the dc voltage $V_d$ ($V_{dM}$) (due to resonance of snubber capacitor with $di/dt$ limiting inductor) before setting down at its steady value $V_d$ . A GTO should not be retriggered within a minimum off period off (min) to avoid the risk of failure due to localized turn ON. GTOs have typically low turn off gain in the range of 4-5.

## 5.4.3  GTO gate drive circuit

A GTO gate drive has to fulfill the following functions.

- Turn the GTO on by means of a high current pulse ($I_{GM}$)

- Maintain conduction through provision of a continuous gate current ($I_G$, also known as the "back-porch current").

- Turn the GTO off with a high negative gate current pulse.

- Reinforce the blocking state of the device by a negative gate voltage.

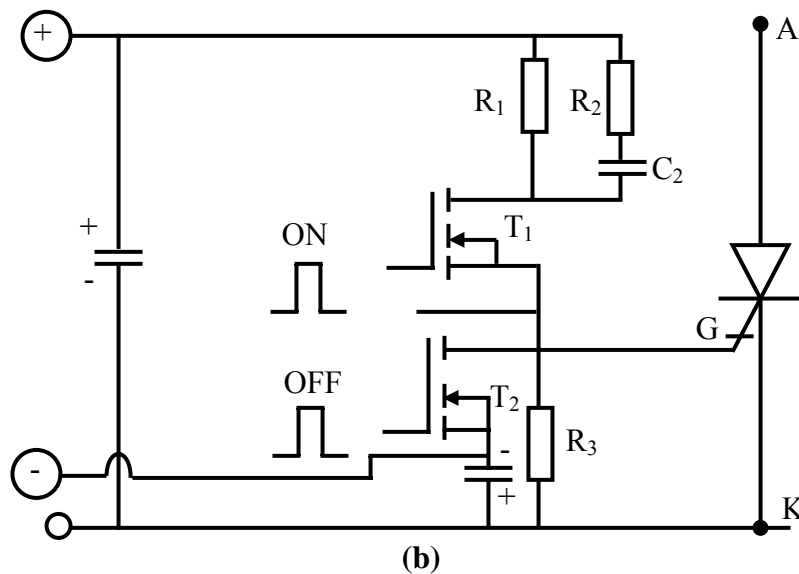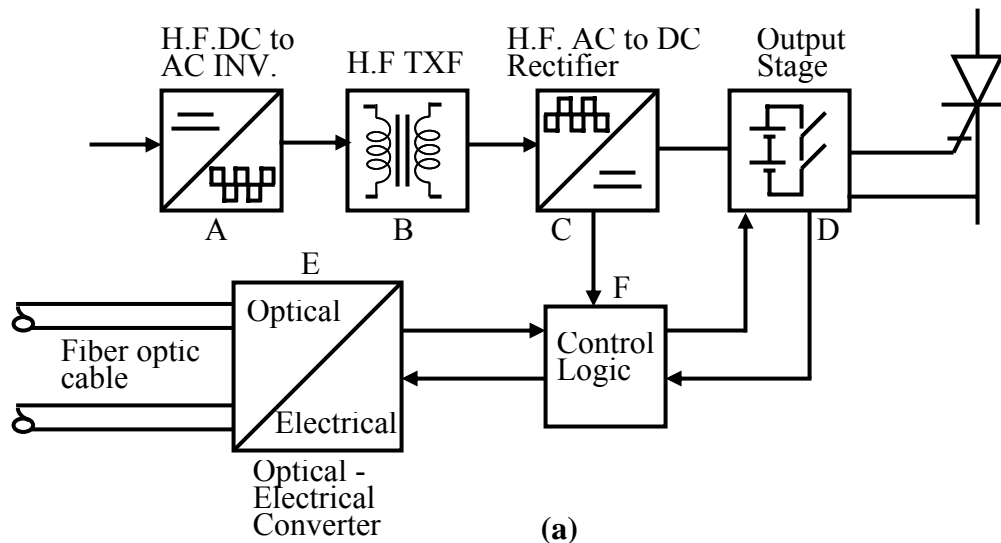A typical gate drive arrangement for a large power GTO is show in Fig 5.5.

**Fig. 5.5:  Gate drive circuit of a GTO.**
**(a) Block diagram,**
**(b) Circuit diagram of the output stage**

In the block diagram of Fig 5.5 (a) it is assumed that there is a potential difference of several kVs between the master control and individual gate units.

The ON and OFF pulses for a GTO is communicated to individual gate units through fiber optic cables. These optical signals are converted to electrical signals by a optical electrical converter. These electrical signals through the control logic then produces the ON and OFF signal for the out put stage which in turn sends positive and negative gate current to the GTO. Depending on the requirement the control logic may also supervise GTO conduction by monitoring the gate-cathode voltage. Any fault is relayed back via fiber optic cable to the master control. Power supply for the Gate drive units are derived from a common power supply through a high frequency SMPS (Blocks A, B & C) arrangement.

Fig 5.5 (b) shows the circuit implementation of the output stage. The top switch $T_1$ sends positive gate pulse to the GTO gate. At the instant of turn on of $T_1$ ,$C_2$ acts almost as a short circuit and

the positive gate current is determined by the parallel combination of $R_1$ and R2. However, at steady state only $R_1$ determines the gate current $I_G$.

The bottom switch $T_2$ is used for biasing the GTO gate negative with respect to the cathode. Since, relatively large negative gate current flows during turn off, no external resistance is used in series with $T_2$. Instead, the ON state resistance of $T_2$ is utilized for this purpose. In practice, a large number of switches are connected in parallel to obtain the required current rating of $T_2$. A low value resistance $R_3$ is connected between the gate and the cathode terminals of the GTO to ensure minimum forward blocking voltage.

**Exercise 5.3**

Fill in the blank(s) with the appropriate word(s)

i.    The _____ current and forward _____ current of a GTO are considerably higher compared to a thyristor.

ii.    If the gate current is insufficient a GTO can operate as a low gain _____.

iii.    Reverse blocking voltage of _____ GTO is small.

iv.    To ensure that all GTO cathode segments are turned on simultaneously the magnitude of the _____ current should be _____.

v.    High value of gate current and dig/dt enhances the _____ capability of a GTO during turn on.

vi.    During storage time the load current in a GTO is diverted from the _____ to the _____ terminal.

vii.    GTOs have low turn off _____ gain.

viii.    After the current fall time during turn off of a GTO the anode current continuous for some more time in the form of a _____.

ix.    The gate drive unit of a GTO should provide continuous positive gate _____ during ON period and continuous negative gate _____ during OFF period.

x.    In the gate drive unit of a GTO a low value resistance is connected between the gate and the cathode terminals to ensure minimum _____ voltage.

**Answer:** (i) latching, leakage; (ii) transistor; (iii) asymmetric; (iv) gate, high; (v) di/dt;
          (vi) cathode, gate; (vii) current; (viii) current tail; (ix) current, voltage; (x)
          forward blocking.

# 5.5  GTO Ratings

## 5.5.1 Steady state voltage and current rating

**V$_{DRM}$:**  It is the maximum repetitive forward voltage the GTO can block in the forward direction assuming line frequency sinusoidal voltage waveform. It is important to note that GTO can block rated voltage only if the gate is reverse biased or at least connected to the cathode through a low value resistance. Manufactures usually provide the forward voltage withstanding capacity of the GTO as a functions of the gate cathode reverse voltage (and /or resistance) for a given forward $\frac{dv}{dt}$ .

**V$_{RRM}$:**  It is the maximum repetitive reverse voltage the GTO is able to withstand. For all asymmetric GTOs this value is in the range of 20-30 V, since it is determined by the gate cathode junction break down voltage. Due to the anode shorted structure of the GTO the anode – base junction (J$_1$) does not block any reverse voltage. Unlike V$_{DRM}$, V$_{RRM}$ rating may be exceeded for a short time without destroying the device. This "reverse avalanche" capability of the GTO is useful in certain situations as explained in Fig 5.6.
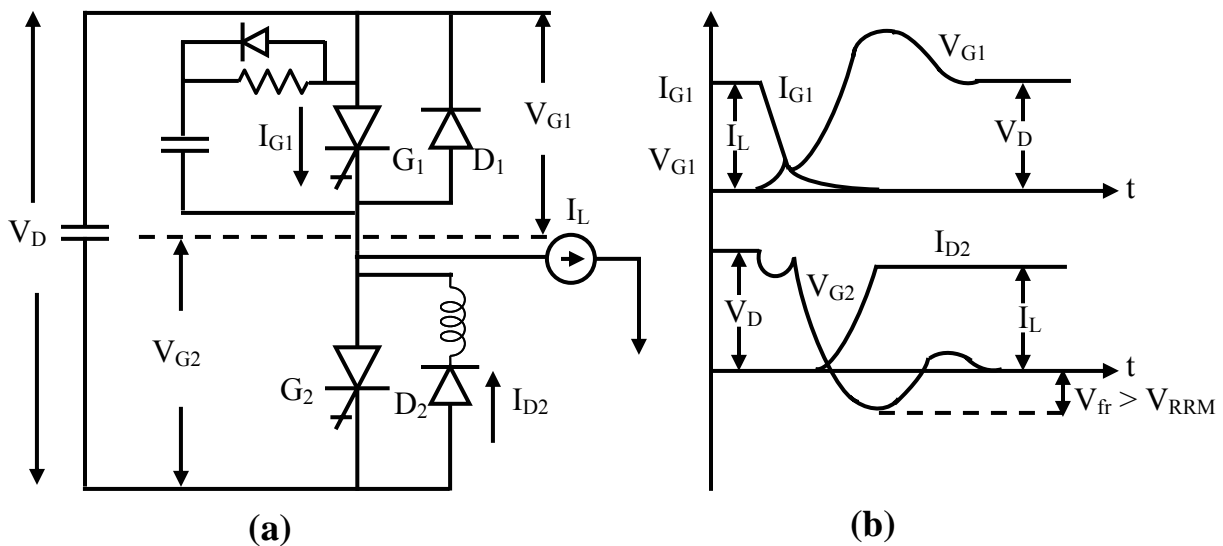


**(a)**                                               **(b)**

**Fig. 5.6:  Reverse avalanche capability of a GTO**
**(a) Voltage source inverter phase leg;**
**(b) Voltage, current waveforms.**

In the voltage source inverter phase leg shown in Fig 5.6 (a), as the GTO G$_1$ is turned off the current through it (I$_{G1}$) starts reducing. The difference current (I$_L$ - I$_{G1}$) is transferred to the snubber capacitance of G$_1$ and the voltage across G$_1$ (V$_{G1}$) starts increasing. When if becomes equal to the dc link voltage V$_D$ , D$_2$ is forward biased. However, due to the forward recovery voltage of D$_2$ (V$_{fr}$) the reverse voltage across G$_2$ may exceed V$_{RRM}$ rating of G$_2$ and drive it into reverse avalanche. This condition is not dangerous for G$_2$ provided the avalanche time and current are small (typically within 10 µs and 1000 A respectively). However, the gate voltage must remain negative during this time.

**V$_{DC}$:**    This is the maximum continuous DC voltage the device can withstand. Exceeding this voltage does not immediately lead to device failure, but the probability of a cosmic radiation failure increases progressively with the applied dc voltage.

**I$_{FAVM}$ and I$_{FRMS}$:**  These are maximum average and RMS on state current respectively. They are specified at a given case temperature assuming half wave sinusoidal on state current at power frequency.

**I$_{FSM}$:**    This is the maximum allowed peak value of a power frequency half sinusoidal non-repetitive surge current. The pulse is assumed to be applied at an instant when the GTO is operating at its maximum junction temperature. The voltage across the device just after the surge should be zero.

**$\int i^2 dt$ :**   This is the limiting value of the surge current integral assuming half cycle sine wave surge current. The junction temperature is assumed to be at the maximum value before the surge and the voltage across the device following the surge is assumed to be zero. The $i^2t$ rating of a semiconductor fuse must be less than this value in order to protect the GTO. Plots of both I$_{FSM}$ and $\int i^2 dt$  as functions of surge pulse width are usually provided by the manufacturer.

**V$_F$ :**    This is the plot of the instantaneous forward voltage drop vs instantaneous forward current at different junction temperatures.

**P$_{av}$ :**    For some frequently encountered current waveforms (e.g. sine wave, square wave) the plot of the average on state power dissipation as a function of the average on state current is provided by the manufacturers at a given junction temperature.

**I$_H$:**    This is the holding current of the GTO. This current, in case of a GTO$_1$ , is considerably higher compared to a similarly rated thyristor. Serious problem may arise due to anode current variation because the GTO may "un-latch" at an in appropriate moment. This problem can be avoided by feeding a continuous current into the gate (called the "back porch" current) during ON period of the device. This DC gate current should be about 20% higher than the gate trigger current (I$_{GT}$) at the lowest expected junction temperature.

**$\dfrac{di}{dt}\big|_{crit}$ :**  This is the maximum permissible value of the rate of change of forward current during turn on. This value is very much dependent on the peak gate current magnitude and the rate of increase of the gate current. A substantial gate current ensures that all GTO cathode segments are turned ON simultaneously and within a short time so that no local hot spot is created. The $di_g/dt$ and I$_{gM}$ values specified in the operating conditions should, therefore, be considered as minimum values.

## 5.5.2  Gate specification

**I$_g$ vs V$_g$:** It is a plot of instantaneous gate current as a function of the gate voltage. This characteristic is valid for DC and low frequency AC gate currents. They do not define the gate

voltage when the GTO is turned on from high anode voltage with high di/dt and $\frac{di_g}{dt}$ . Vg in this case is much higher. Generally the gate cathode impedance of a GTO is much lower than that of a conventional thyristor.

**$V_{gt}$, $I_{gt}$:** $I_{gt}$ is the gate trigger current and $V_{gt}$ , the instantaneous gate cathode voltage when $I_{gt}$ is flowing into the gate. $I_{gt}$ has a strong junction temperature dependence and increases very rapidly with reduced junction temperature. $I_{gt}$ merely specifies the minimum back porch current necessary to turn on the GTO at a low $\frac{di}{dt}$ and maintain it in conduction.

**$V_{grm}$:** It is the maximum repetitive reverse gate voltage, exceeding which drives the gate cathode junction into avalanche breakdown.

**$I_{grm}$:** It is the peak repetitive reverse gate current at $V_{grm}$ and $T_j$ (max).

**$I_{gqm}$:** It is the maximum negative turn off gate current. The gate unit should be designed to deliver this current under any condition. It is a function of turn off anode current, $\frac{di_g}{dt}$ during turn off and the junction temperature.

## 5.5.3  Specifications related to the switching performance

**$t_d$, $t_r$, :** These are turn on delay time and anode voltage fall time respectively. Both of them can be reduced with higher $\frac{di_g}{dt}$ and $I_{gM}$ for a given turn on anode voltage, current and $\frac{di}{dt}$ .

**$t_{on}$ (min) :** This is the minimum time the GTO requires to establish homogeneous anode current. This time is also necessary for the GTO to be able to turn off its rated anode current.

**$E_{ON}$ :** It is the energy dissipated during each turn on operation. Manufacturers specify them as functions of turn on anode current for different turn on di/dt and anode voltage $E_{ON}$ reduces with increased $I_{gM}$ .

**$I_{Fgqm}$ :** It is the maximum anode current that can be repetitively turned off by a negative gate current. It can be increased by increasing the value of the turn off snubber capacitance which limits the dv/dt at turn off. A large negative dig/dt during turn off also helps to increase $I_{Fgqm}$.

**$t_s$ :** The storage time $t_s$ is defined as the time between the start of negative gate current and the decrease in anode current. High value of the turn off anode current and junction temperature increases it while a large negative dig/dt during turn off decreases it.

**$t_f$ :** This is the anode current fall time. It can not be influenced much by gate control.

**$t_{off}$(min) :** This is the minimum off time before the GTO may be triggered again by a positive gate current. If the device is re-triggered during this time, localized turn on may destroy it.

**E$_{off}$:**  This is the energy dissipated during each turn off operation of the GTO. E$_{off}$ increases with increase in the turn off anode current and junction temperature while it reduces with turn off snubber capacitance.

**Exercise 5.4**

Fill in the blank(s) with the appropriate word(s)

 i. A GTO can block rated forward voltage only when the gate is _____ biased with respect to the _____.

 ii. A GTO can operate in the reverse _____ region for a short time.

 iii. The holding current of a GTO is much _____ compared to a thyristor.

 iv. After a current surge the voltage across a GTO should be reduced to _____.

 v. The gate cathode impedance of a GTO is much _____ compared to a thyristor.

 vi. The turn on di/dt capability of a GTO can be increased by in creasing the _____ magnitude of the gate current and _____ during turn on.

 vii. The turn on delay time and current rise time of a GTO can be reduced by increasing the gate current _____ and _____ during turn ON.

 viii. The maximum anode current that can be turned off repetitively can be increased by increasing the turn off snubber _____ and negative _____.

**Answer:** (i) negatively, cathode; (ii) avalanche; (iii) larger; (iv) zero; (v) smaller; (vi) peak, dig/dt; (vii) magnitude, dig/dt; (viii) capacitance, dig/dt.


# Reference

1) "GTO and GCT product guide", ABB semiconductors AG, 1997.
2) "GTO Thyristors" , Makoto Azuma and Mamora Kurata, Proceedings of the IEEE, Vol.76, No. 4, April 1988, pp 419-427.
3) "Power Electronics", P. S. Bimbhra, Khanna Publlishers, 1993.

# Lesson Summary

- GTO is a four layer, three terminal current controlled minority carrier device.

- A GTO can be turned on by applying a positive gate current pulse when it is forward biased and turned off by applying a negative gate current.

- A GTO has a "shorted anode" and highly inter-digitized gate cathode structure to improve the gate turn off performance.

- Due to the presence of "anode shorts" a GTO can block only a small reverse voltage. These are called "asymmetric GTOs".

- The forward i-v characteristics of a GTO is similar to that of a thyristor. However, they have relatively larger holding current and gate trigger current.

- The turn on di/dt capability of a GTO is significantly enhanced by using higher peak gate current and large rate of rise of the gate current.

- Due to relatively larger holding current of a GTO a continuous low value gate current (called the back porch current) should be injected through out the on period of the GTO.

- GTOs have relatively low turn off current gain.

- The GTO gate drive unit should be capable of injecting large positive and negative gate currents with large rate of rise for satisfactory switching of the device.

- A GTO can block rated forward voltage only when the gate cathode junction is reverse biased.

- A GTO can operate safely in the "reverse avalanche" region for a short time provided the gate cathode junction is reverse biased.

- The switching delay times and energy loss of a GTO can be reduced by increasing the gate current magnitude and its rate of rise.

- The maximum turn off anode current of a GTO can be increased by increasing the turn off snubber capacitance.

# Practice Problems and Answers

1. What are the constructional features of a GTO that bestows it with a gate turn off capability? How do they affect the turn on performance of the GTO?

2. What are the main differences in the steady state output characteristics of a GTO and a thyristor? What effect do they have on the gate drive requirement of a GTO?

3. What are the desirable characteristics of the gate drive circuit of a GTO? How do they influence the switching performance of a GTO?

4. What is the significance of the specifications $I_{FAVM}$ and $I_{FRMS}$ in relation to a GTO? Is the specification $I_{Fgqm}$. Same as $I_{FAVM}$ / $I_{FRMS}$? If not, then which current should one use in a particular application?

5. Which paramers of the gate current waveform reduces the turn on energy loss ($E_{ON}$) of a GTO? How does one reduce the turn off energy lass of a GTO?

# Answers to practice problems

1. Although a GTO is a four layer (**p-n-p-n**) three junction devices like a thyristor it has two important constructional differences with a thyristor which bestows it with the gate turn off capability.

- The Gate-cathode junction of a GTO is far more inter digitized compared to a thyristor. Thousands of cathode segments, normally arranged in concentric rings around the device center, from the cathode structure of a GTO. This highly inter digitized structure of the GTO cathode ensures that any "current filament" formed during the turn off process of a GTO is quickly extinguished.

- "Anode shorts" are introduced at the **p+** type anode and **n** type base junction of a GTO. "Anode shorts" consists of heavily doped **n+** type region introduced inside the **p+** type anodes. They make direct contact with the anode metal plate and provide an alternate path for the electrons traveling through the **n** base to reach the anode metal contact without causing bole injection from the **p+** anode. This helps to reduce the "tail current" during turn off of a GTO.

- Highly inter digitized gate-cathode structure of a GTO helps to enhance the turn on di/dt capability of the device due to faster and more even spreading of the injected gate current to adjacent cathodes.

- On the other hand, presence of anode shorts has adverse effect on the turn on performance of a GTO. Referring to Fig 5.2 (a), introduction of anode shorts effectively reduces the current gain ∝p of the top **p-n-p** transistor. This has the effect of increasing the latching and holding current of a GTO compared to a thyristor. The minimum gate current required to trigger a GTO also increases.

2. In the first quadrant of the output i-v plane the steady state output characteristics of a GTO appears to be similar to that of a thyristor. There are some important differences however.

- Both holding and latching current of a GTO are considerably higher compared to a similarly rated thyrisstor.

- The minimum gate current require to trigger a GTO at a given forward blocking voltage is higher compared to a thyristor.

- The forward leakage current of a GTO is considerably higher compared to a thyristor of equal rating. In fact, if the gate current is not sufficient to turn on a GTO it may operate as a high voltage low gain transistor with considerable anode current.

- A GTO can block rated forward voltage only when the gate voltage is negative with respect to the cathode or at least the gate is connected to the cathode through a low value resistance.

- In the reverse blocking region (i.e third quadrant of the output i-v plane) an asymmetric GTO has much lower reverse break down voltage (20-30V) compared to a thyristors. Exceeding this reverse voltage forces the GTO to operate in the "reverse avalanche" mode.

This mode of operation does not destroy the device provided the gate is negatively biased and the time of such operation is small.

- Since the holding current of a GTO is considerably higher than that of a thyristor anode current variations can generate serious problem because the GTO might "unlatch" at an inappropriate moment. To avoid this problem the gate drive unit of a GTO must feed the gate terminal with a continuous "back porch" current during the entire on period of the GTO. This back porch current must be larger than the gate trigger current.

- To avoid localized transistor operation during turn on from a high anode voltage with large di/dt, the gate drive unit must inject a peak gate current considerably larger (3-10 times) than the gate trigger current with fast rate of rise.

- To ensure that the GTO blocks rated forward voltage and operates safely in the "reverse avalanche" mode the gate voltage must be maintained negative with respect to the cathode for the entire off duration of the GTO.

3. The gate drive unit of a GTO should.

- Turn the GTO on with a large (3-10 times the minimum gate trigger current) positive gate current pulse with high rate of rise.

- Maintain conduction of the GTO through out the ON period by injecting a positive "back porch" gate current which is larger than the minimum gate trigger current.

- Turn the GTO off with a large negative gate current with high rate of fall. The peak magnitude of the negative gate current should be at least 20-25% of the maximum anode current during turn off.

- Reinforce the blocking state of the device by applying a negative voltage to the gate with respect to cathode for the entire off duration of the GTO.

  Both the turn on delay time ($t_d$) and the voltage fall time ($t_r$) of a GTO can be reduced by increasing the peak positive gate current and its rate of rise during turn on. Energy loss per turn on ($E_{ON}$) also reduces.

  A large negative gate current during turn off with a stiff slope considerably reduces the storage time ($t_s$) and enhances maximum anode current turn off ($I_{Fgqm}$) capability.

4. The specifications of $I_{FAVM}$ and $I_{FRMS}$ are given with reference to power frequency half cycle sine wave anode current. If the GTO is employed in a line commutated phase controlled converter application then these specifications give the maximum allowable average and RMS current through the device respectively. However, in most GTO applications the current waveform is for removed from a sinusoidal shape and the switching losses are a considerable part of the total power losses. $I_{FAVM}$ / $I_{FRMS}$ ratings, in such cases, does not have any practical significance except for comparison of current carrying capacity of different devices.

  On the other hand, $I_{Fgqm}$ rating of a GTO gives the maximum anode current that can be repetitively turned off by gate control. This rating is usually lower than $I_{FAVM}$ / $I_{FRMS}$. In

high frequency switching application this specification gives the absolute peak value of any desired current waveform the GTO can conduct.

5. $E_{on}$ is reduced by increasing the peak magnitude of the positive gate current during turn on. $E_{off}$ is reduced by increasing the turn off snubber capacitance across the GTO.