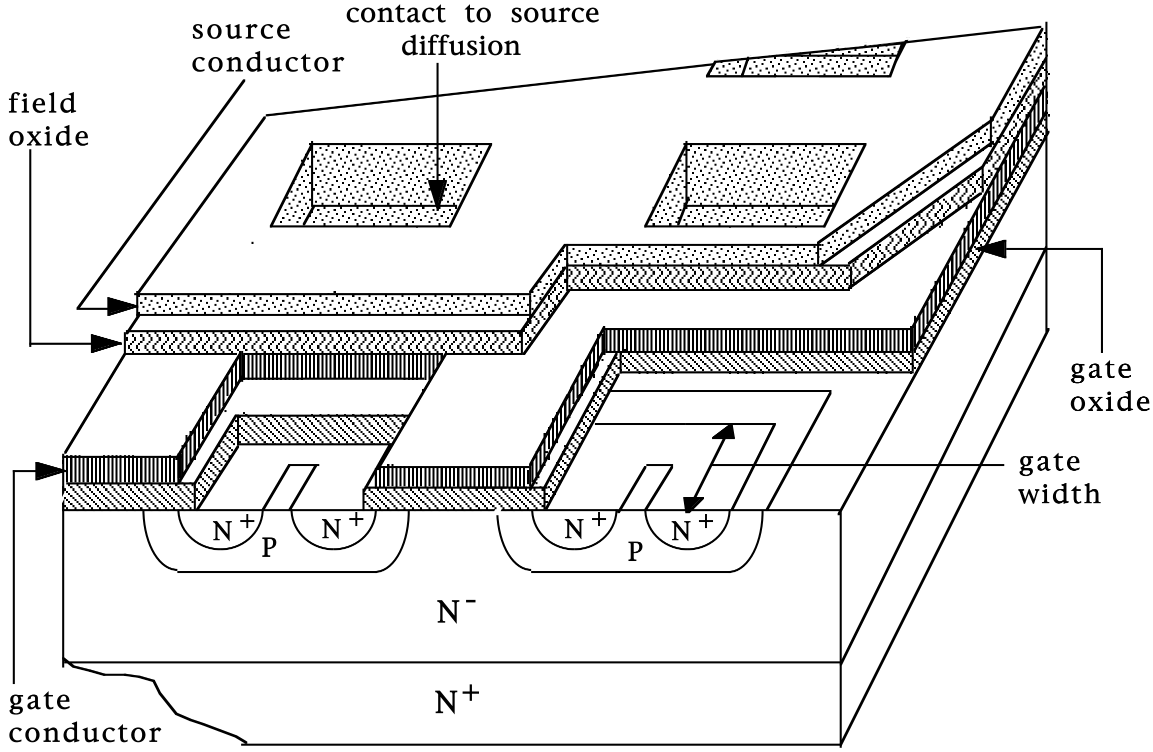
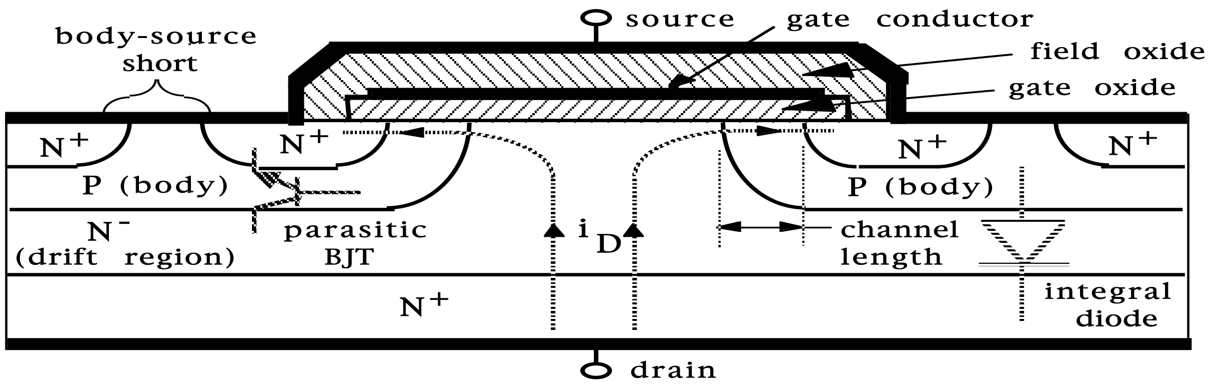
Multi-cell Vertical Diffused Power MOSFET (VDMOS)

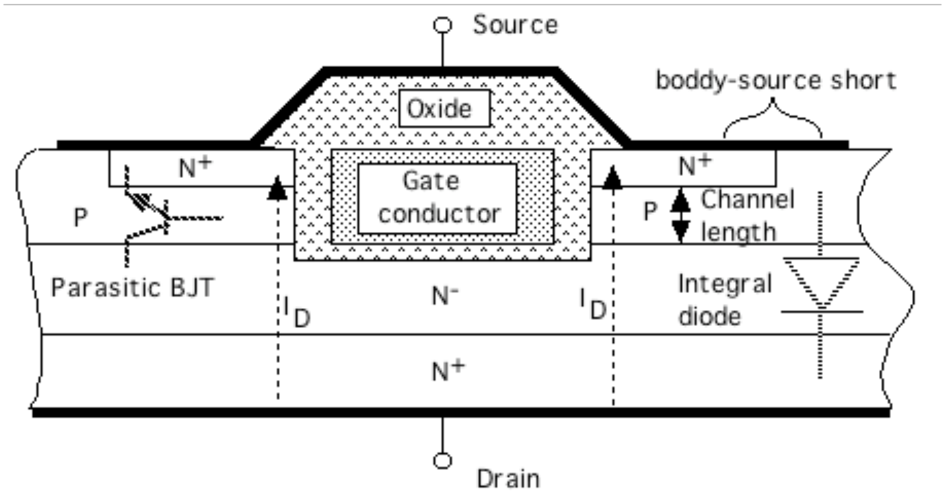


Important Structural Features of VDMOS

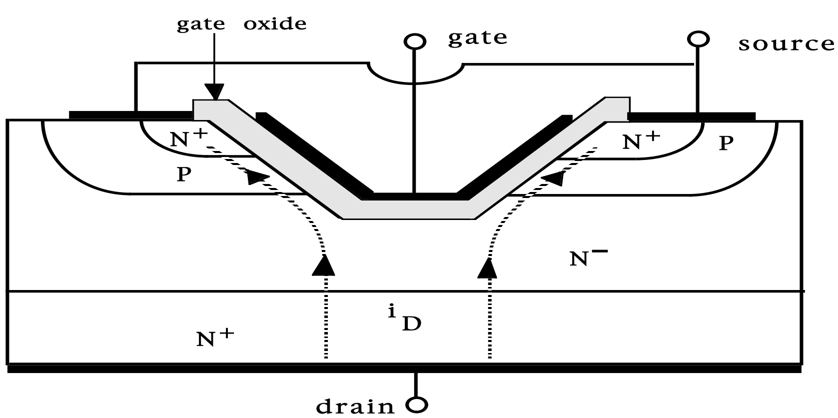


1. Parasitic BJT. Held in cutoff by body-source short
2. Integral anti-parallel diode. Formed from parasitic BJT.
3. Extension of gate metallization over drain drift region. Field plate and accumulation layer functions.
4. Division of source into many small areas connected electrically in parallel. Maximizes gate width-to-channel length ratio in order to increase gain.
5. Lightly doped drain drift region. Determines blocking voltage rating.

Alternative Power MOSFET Geometries

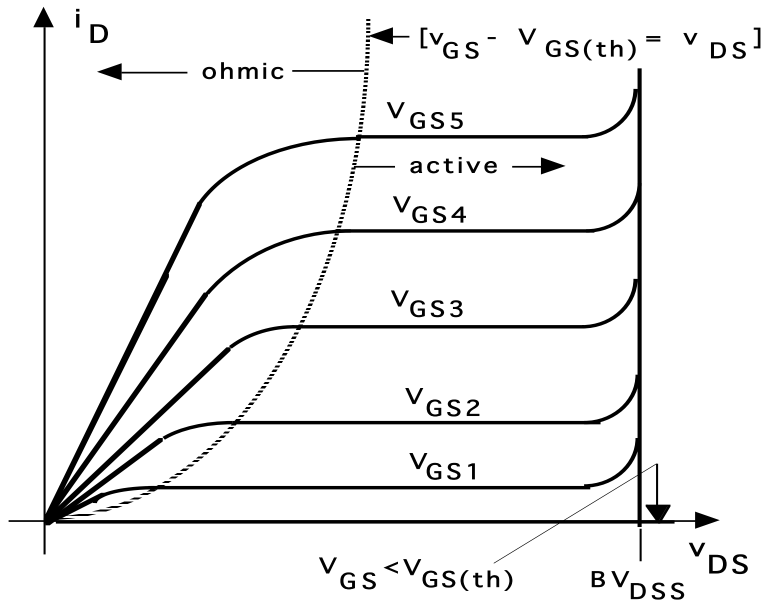


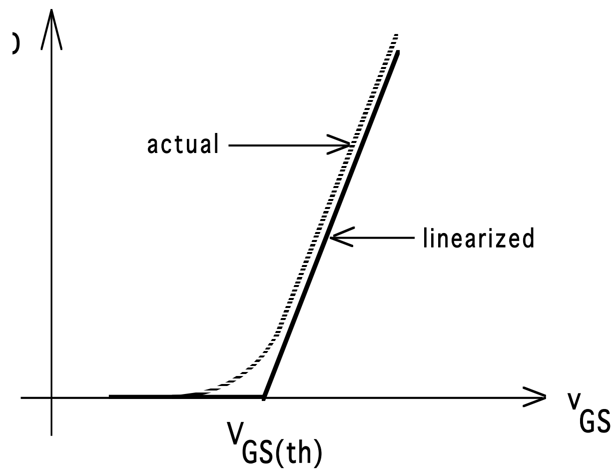
- Trench-gate MOSFET
- Newest geometry. Lowest on-state resistance.

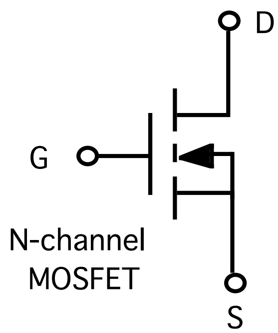


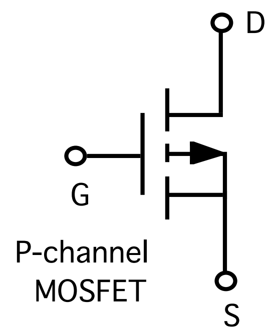
- V-groove MOSFET.
- First practical power MOSFET.
- Higher on-state resistance.

MOSFET I-V Characteristics and Circuit Symbols

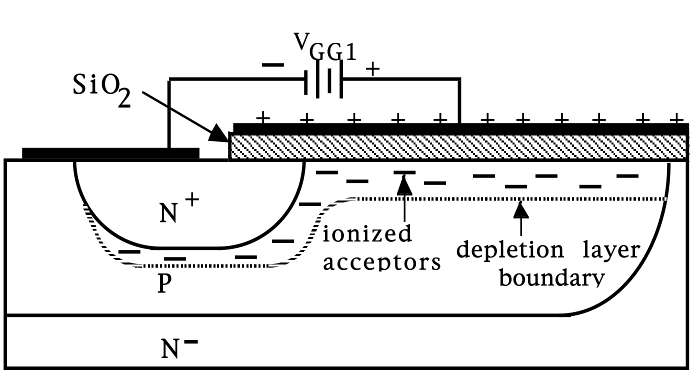


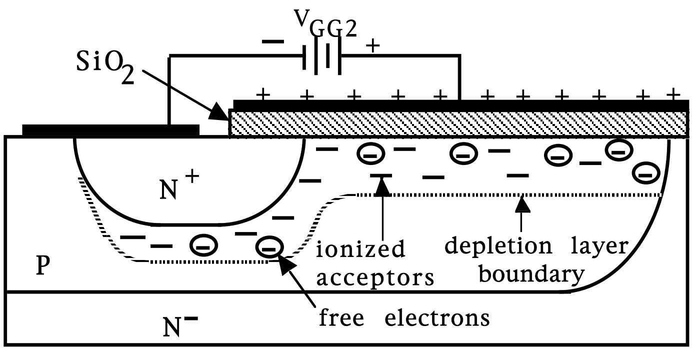






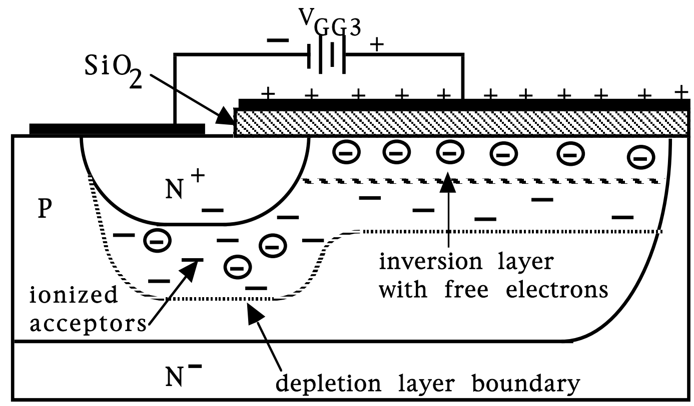
The Field Effect - Basis of MOSFET Operation





Threshold Voltage $V_{GS(th)}$

- V_{GS} where strong inversion layer has formed. Typical values 2- 5 volts in power MOSFETs

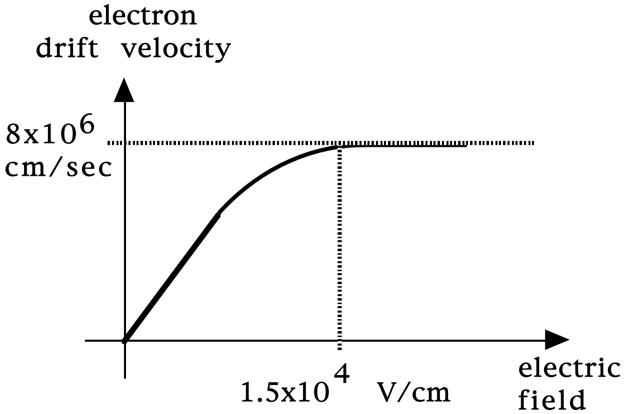


- Value determined by several factors
  1. Type of material used for gate conductor
  2. Doping density of body region directly beneath gate
  3. Impurities/bound charges in oxide
  4. Oxide capacitance per unit area $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

     t_{ox} = oxide thickness

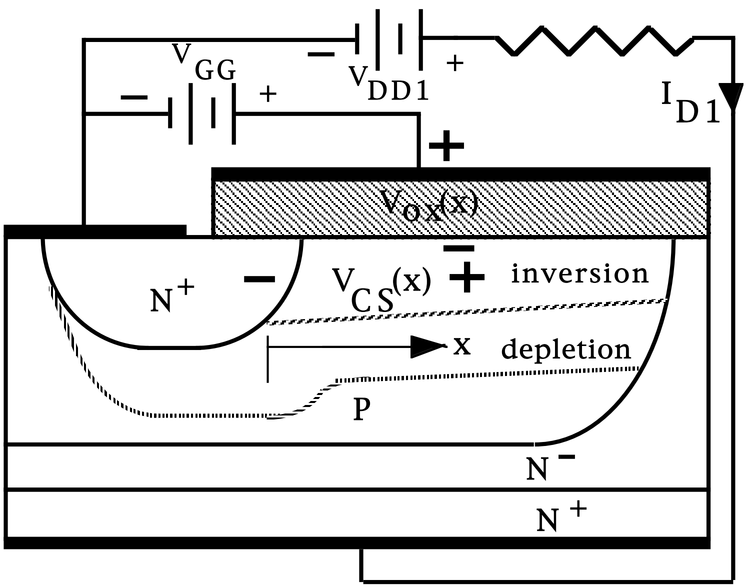
- Adjust threshold voltage during device fabrication via an ion implantation of impurities into body region just beneath gate oxide.

Drift Velocity Saturation



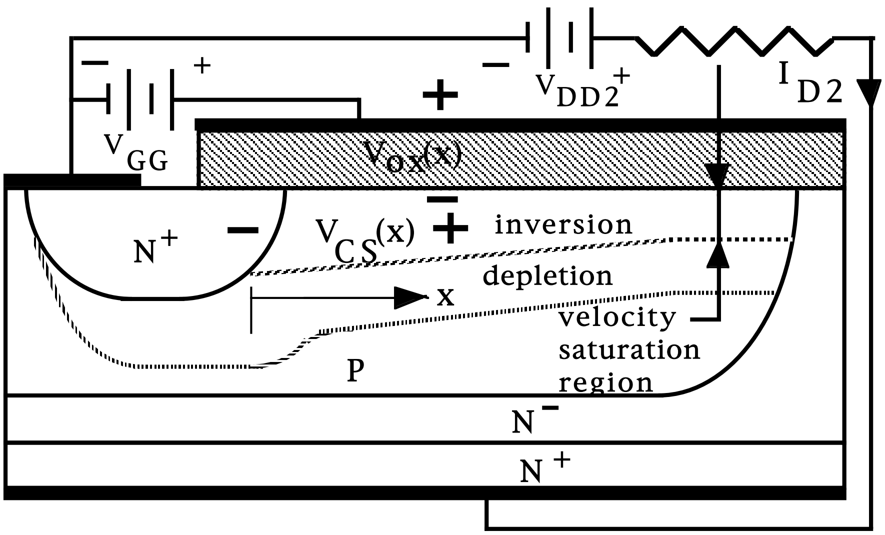
- In MOSFET channel, $J = q \mu_n n E = q n v_n$; velocity $v_n = \mu_n E$
- Velocity saturation means that the mobility μ_n inversely proportional to electric field E.
- Mobility also decreases because large values of V_{GS} increase free electron density.
- At larger carrier densities, free carriers collide with each other (carrier-carrier scattering) more often than with lattice and mobility decreases as a result.
- Mobilty decreases, especially via carrier-carrier scattering leead to linear transfer curve in power devices instead of square law transfer curve of logic level MOSFETs.

Channel-to-Source Voltage Drop



- $V_{GS} = V_{GG} = V_{ox} + V_{CS}(x)$;
  $V_{CS}(x) = I_{D1} R_{CS}(x)$
- Larger x value corresponds be being closer to the drain and to a smaller V_{ox}.
- Smaller V_{ox} corresponds to a smaller channel thickness. Hence reduction in channel thickness as drain is approached from the source.

Channel Pinch-off at Large Drain Current



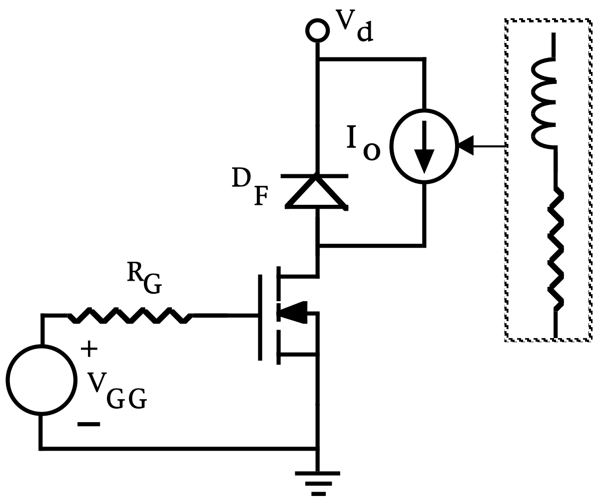
- $I_{D2} > I_{D1}$ so $V_{CS2}(x) > V_{CS1}(x)$ and thus channel narrower at an given point.
- Total channel resistance from drain to source increasing and curve of I_D vs V_{DS} for a fixed V_{GS} flattens out.

- Apparent dilemma of channel disappearing at drain end for large I_D avoided.

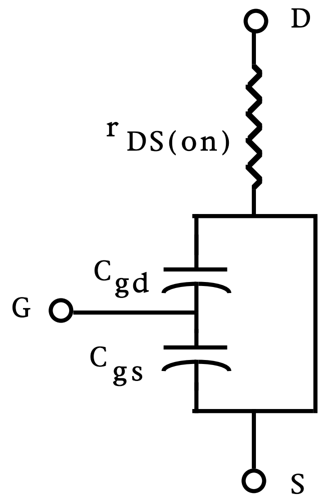
1. Large electric field at drain end oriented parallel to drain current flow. Arises from large current flow in channel constriction at drain.
2. This electric field takes over maintenance of minimum inversion layer thickness at drain end.

- Larger gate-source bias V_{GG} postpones flattening of I_D vs V_{DS} until larger values of drain current are reached.

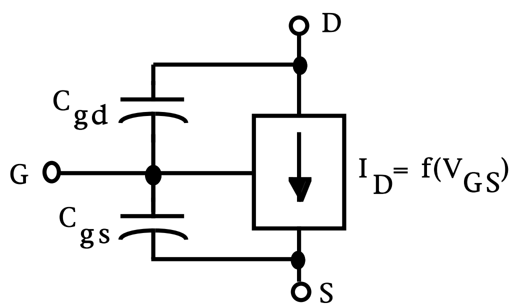
MOSFET Switching Models for Buck Converter



• Buck converter using power MOSFET.

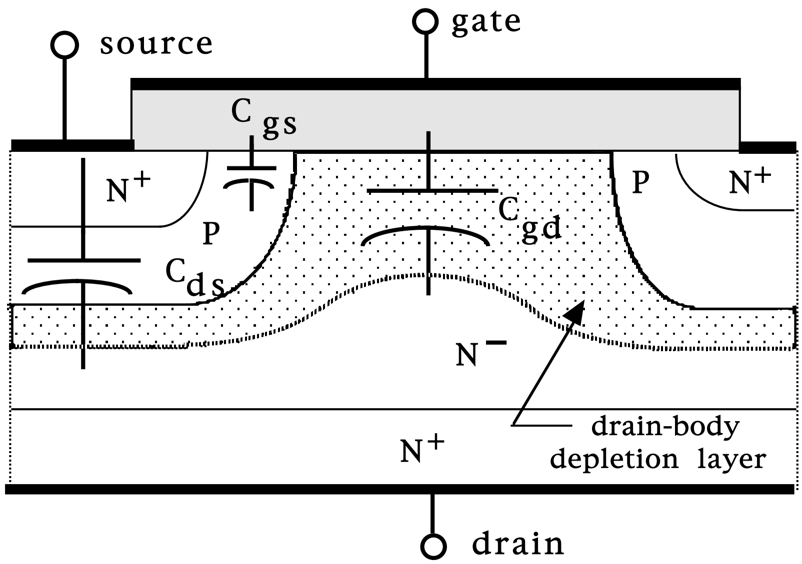


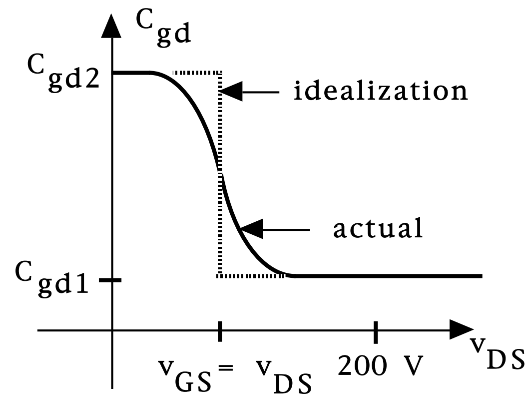
• MOSFET equivalent circuit valid for on-state (triode) region operation.



• MOSFET equivalent circuit valid for off - state (cutoff) and active region operation.

MOSFET Capacitances Determining Switching Speed





- Gate-source capacitance Cgs approximately constant and independent of applied voltages.

- Gate-drain capacitance C_{gd} varies with applied voltage. Variation due to growth of depletion layer thickness until inversion layer is formed.